EE/CprE/SE 491 WEEKLY REPORT 9

11/8/2024 - 11/14

Group number: sdmay25-19

Project title: ReRAM AI Accelerator

Client &/Advisor: Dr. Henry Duwe and Dr. Cheng Wang

Team Members/Role: Noah Mack, Olivia Price, Sam Burns, Travis Jakl

- **Weekly Summary**

Travis has been leading the way and doing a great job testbenching and reporting on each of the previous team's modules. The rest of the group has been working on getting through precheck with the inverter, but has also started taking a look at and benchmarking the previous team's modules.

- **Past week accomplishments**

  • Sam Burns: Worked on addressing persistent LVS issues with digital harness. Reached out to the efabless team via the open-source silicon slack channel. Worked on comparing architectures of past teams to each other for our architecture document.

  • Travis Jakl: Worked on finishing testbenching and reporting on each of the modules. Also made a github repo for my teammates to have an initialized reram cell setup

  • Noah Mack: Stopped my precheck from throwing an exception based on Travis' suggestion. Kept working on trying to pass all the checks. Worked with Dr. Duwe to revise design document.

  • Olivia Price: Continued working through the inverter tutorial. Also started working on taking a look at the previous team's modules and began checking out their testbenches.

- **Pending issues**

  • Sam Burns: LVS issue with digital harness, I have reached out to the efabless team via slack

  • Travis Jakl: N/A

  • Noah Mack: Still getting through precheck, but precheck is not erroring out anymore

  • Olivia Price: Just getting through the inverter

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**

Sam Burns	Looked over past teams architectures. Introduced myself to the efabless team on Slack	6	64
Travis Jakl	Finished testbenching and reporting on modules. Made a github repo	6	59
Noah Mack	Fixed the bug with precheck based on Travis' suggestion. Revised and got feedback from Dr. Duwe about design document.	6	65
Olivia Price	Almost done with inverter, still running into some issues. Started looking into the previous team's modules a little bit.	6	64

- **<u>Plans for the upcoming week</u>**

  • Sam Burns: Get through precheck with the digital harness, take layout of past team through precheck (minus the ReRAM cells).

  • Travis Jakl: Start making my own testbenches for modules that do not currently exist.

  • Noah Mack: Get through precheck with the digital harness, help Travis make testbenches for modules. Also look into adding section to design document as advised by Dr. Duwe.

  • Olivia: Finish up inverter, then start working on the previous team's modules to get testbenches created and get it through precheck

- **<u>Summary of weekly advisor meeting</u>** (*If applicable/optional)*

  This week, we revised our design section of our design document since we were unable to go over it with our advisors last week since it was not done yet. They gave some good revision suggestions, and talked about adding quantitative details to many parts of the document. Dr. Duwe also specifically had the idea of comparing Noah's quantization accuracy numbers from his CprE 487 class with the ADC precision coming out of our ReRAM architectures to give quantitative estimates of accuracy loss with loss of precision.