***EE/CprE/SE 491 WEEKLY REPORT 7***

***10/18/2024-10/24/2024***

***Group number: sdmay25-19***

***Project title: ReRAM AI Accelerator***

***Client &/Advisor: Dr. Henry Duwe and Dr. Cheng Wang***

***Team Members/Role: Noah Mack, Olivia Price, Sam Burns, Travis Jakl***

- **Weekly Summary**

  We are in the final week of our first task of working through each stage of the analog toolflow and updating tutorial documentation on the CHIP Forge website. We are at various stages of finishing the analog toolflow with some of us being done, and others getting closer. Once this week is over we will begin verifying the designs of past teams, looking at testbench simulations and layouts.

- **Past week accomplishments**

  • Sam Burns: Worked on getting our inverter design integrated into a digital harness and fixed DRC errors on the design. Attempted to fix issues with LVS as well.

  • Travis Jakl: Properly installed the ReRAM cell, made sure that it was functioning properly, and then started to look into the first ReRAM teams testbench cases to ensure those are functioning as they should

  • Olivia Price: Finishing up the tutorial on creating an inverter and getting it through pre-check. However, I am having problems putting the final inverter layout into the empty wrapper.

  • Noah Mack: Worked on integrating the inverter design into the top level diagram. Made the layout and attempted LVS.

- **Pending issues**

  • Sam Burns: Struggling to address issues with LVS on digital harness

  • Travis Jakl: Figure out what to do about the missing files from the first ReRAM's testbenches

  • Olivia Price: Struggling to get the inverter in the wrapper

  • Noah Mack: LVS failing for top level wrapper

- **Individual contributions**

| **NAME** | **Individual Contributions** *(Quick list of contributions. This should be short.)* | **Hours this week** | **HOURS cumulative** |
|---|---|---|---|

| | | | |
|---|---|---|---|
| Sam Burns | Finished integrating inverter into digital harness<br>Fixed DRC errors with design<br>Worked to eliminate outstanding LVS issues | 6 | 53 |
| Travis Jakl | Installed ReRAM cell<br>Properly tested and simulated the ReRAM cell<br>Investigated first ReRAM team's testbenches | 6 | 53 |
| Olivia Price | Finished simulating the inverter in layout and schematic. Trying to get the inverter into the wrapper. | 6 | 52 |
| Noah Mack | Finished layout for top level wrapper, tried running LVS | 6 | 59 |

- **Plans for the upcoming week**

• Sam Burns: Get inverter through LVS errors and then precheck, start evaluating old teams design and look at testbenches. We will also develop testbenches on modules that don't have test benches

• Travis Jakl: Continue to work with the testbenches that are available and create new testbenches to test modules that dont have testbenches

• Olivia Price: Finish the inverter, get it through LVS and pre-check. Then hopefully, start looking at old ReRAM architectures and start designing new ones. Making some block diagrams for our client to look over.

• Noah Mack: Finish the inverter and then start working on testing the previous team's component circuitry.

- **Summary of weekly advisor meeting**

Most of our work at our weekly meeting focused on making revisions to our design document and establishing rules for how we upload our work using git. We focused on task decomposition and project management procedures. We also talked about how to change the format of our risk management section.