EE/CprE/SE 491 WEEKLY REPORT XY

10/18/2024-10/24/2024

Group number: sdmay25-19

Project title: ReRAM AI Accelerator

Client &/Advisor: Dr. Henry Duwe and Dr. Cheng Wang

Team Members/Role: Noah Mack, Olivia Price, Sam Burns, Travis Jakl

- **Weekly Summary**

This week, our group continued working together on our individual basic inverter projects. Travis successfully got his design through pre-check! Other members in the group are still working through the process, but everyone has made progress. We also made some improvements to our ongoing design document, with the help of Dr. Duwe and Dr. Wang.

- **Past week accomplishments**

  • Noah Mack: Worked on my inverter project. Designed my layout, which I had never done before, and got through LVS; now working on my layout of my top level design.

  • Sam Burns: I was able to get my program to successfully generate a SPICE file from the schematic and get an inverter through LVS.

  • Travis Jakl: I was able to successfully get the inverter all the way through precheck, resolving the GPIO define issues, as well as the LVS issues.

  Olivia Price: I was able to figure out why I couldn't generate a testbench properly. I also ran into another issue with not being able to do LVS check but then Travis helped me on that today. Hopefully, I can get the inverter done soon.

- **Pending issues** *(If applicable: Were there any unexpected complications? Please elaborate.)*

  •Noah Mack: Today, my LVS failed when trying to run my top level design through LVS. Haven't looked into it too much yet since it just happened today.

  • Sam Burns: I am having a new issue with SPICE file generation. This time it failed to include the instance of the inverter in the SPICE file when trying to simulate the circuit after parasitic extraction. Numerous attempts were made to resolve the issue but no success.

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- **Individual contributions** *(Creating this section is optional, but it is **Required to include the "Hours Worked for the Week" and their "Total Cumulative Hours" for the project for each member somewhere relevant in your report. Your individual weekly hours should be at a minimum of 6-8 hours for this course. So please manage your time well. Also, ensure that individual contributions support your claim to the weekly hours. Be honest with the reports.**)*

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Noah Mack	Worked on my inverter project and contributed to the design document.	6	47
Sam Burns	Worked fixing issue with circuit simulation, then did the layout and lvs of the inverter.	6	47
Travis Jakl	Worked towards getting the inverter through precheck by resolving the GPIO Define issues and LVS issues	6	47
Olivia Price	Worked on getting the inverter through LVS check, and overcame other issues in the process.	6	47

- **Plans for the upcoming week**

  • Noah Mack: Continue working through my inverter project. After that, I will join Travis in starting to test the previous teams' circuits that we will be working off of.

  • Sam Burns: Get inverter through precheck. Begin simulation and verification of a past teams design

  • Travis Jakl: With a complete precheck accomplished, I will begin navigating modules from the first ReRAM team, test benching their individual components and making sure that they function properly.

  • Olivia Price: Hopefully get the inverter done and all the way through pre-check. Then start working on past team's projects and see if they can pass all of LVS and pre-check.

- **Summary of weekly advisor meeting**

This week in our advisor meeting, we talked about some issues that we were having in our design process. Dr. Duwe suggested that we ask a question on the open source silicon slack channel, which we will definitely pursue in the future. Dr. Duwe and Dr. Wang also helped us refine our requirements and constraints in our design document.