EE/CprE/SE 491 WEEKLY REPORT 1

September 27th – October 3, 2024

Group number: sdmay25-19

Project title: ReRAM AI Accelerator

Client &/Advisor: Dr. Henry Duwe and Dr. Cheng Wang

Team Members/Role: Noah Mack, Olivia Price, Sam Burns, Travis Jakl

- **Weekly Summary**

  This week our team tried to make some edits to our existing design document to better represent our goal as a team and to effectively communicate our problems, user needs, and requirements. We also began working to make a project of our own in xschem that we want to take all the way through precheck. However, each of us ran into an issue at different points in the process.

- **Past week accomplishments**

  • Sam Burns: Created a clone of a Caravel project template from the efabless website to try and fix the spice file generation issues. This did fix the issue but new issues arose when trying to simulate a simple inverter.

  • Travis Jakl: Continued to work on running the inverter to a final precheck. Fixed the final LVS issue that was occurring, and have resolved ⅗ precheck failures

  • Olivia Price: Followed the 80 page document until I got stuck, then tried to get unstuck but its not working, so I will be trying to redownload the package.

  • Noah Mack: Finally made headway on getting the inverter project to run from the blank template. I successfully troubleshooted the tool issues I was having and was able to simulate my inverter that I made from scratch.

- **Pending issues**

  • Sam Burns: Spice models of the sky130 process components seem to be missing in my cloned project.

  • Travis Jakl: Precheck failures (GPIO Defines, LVS, maybe Consistency?)

  •Olivia Price: schematic could not create a raw file

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Sam Burns	- Fixed SPICE file generation issue - Ran into simulation error - Tried copying dependencies folder from original project with no success	6	41
Travis Jakl	- Resolved final LVS issues - Run precheck and fixed at least 2 issues with at least 2 remaining	6	41
Olivia Price	- Trying to follow the 80 page document	6	36
Noah Mack	- Succeeded in simulating inverter schematic	6	41

- **Plans for the Upcoming Week**

  ·Sam Burns: Iron out the simulation issues I am having after cloning a new caravel template, I will also work through the layout. Passing DRC and LVS. We will also discuss plans for our own designs.

  · Travis Jakl: Finish the precheck fixes, once the final precheck has been successfully ran and the errors understood, I will begin to work on testing previous teams modules and subsystems

  • Olivia Price: Try to get the 80-page tutorial done, download a ReRAM cell, and get the testbench working. Look at past teams designs and try to integrate them.

  · Noah Mack: Continue with my inverter project and work towards getting it through pre-check

- **Summary of weekly advisor meeting:**

During this weekly advisor meeting, our advisor tried to help us troubleshoot some of the errors that we were getting for pre-check. Then we looked over our design documents' problem statement and user needs to refine and fix so they fit our advisor/client needs. Lastly, we talked about plans for next week and that we should try to get the pre-check done and start looking over the past team's designs.