ASIC Design of ReRAM-based AI Accelerators

Design Document

Sdmay25-19
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Executive Summary

When you enter a mathematical problem into a computer, the data must be stored in memory and then travel to the arithmetic logic unit (ALU) and back to memory. This process consumes a lot of power and takes time. This begs the question, is there a solution that can be created with existing technology. A solution that can perform matrix-vector multiplication (MVM) in the memory unit? This project focuses on finding a way to implement ReRAM, an upcoming memristor storage cell for data that can perform MVM.

The key requirements for this project are to have four different working ReRAM architectures that can be tested individually on a test chip. In previous semesters, there were two groups who worked on this project, and each created a design, so our team needed to implement two more designs to place on the final chip. With our two new designs, we need to implement C-code for the MCU to interface with the ReRAM cells. Lastly, this project should be concluded before April 21st, 2025, the tape-out date.

The two designs we have decided to implement that are unique from the other groups are within the ReRAM cell. The first design is instead of having the word line and source line parallel, it will be the bit line and sources line aligned. Our second design is to get rid of the transistor altogether and implement a true ReRAM crossbar, which just entails the memristor. In order to execute these designs, we will be following the Skywater 130nm process and using open-sourced technology to create our circuits, layouts, and perform testing. The open-sourced technology includes Xschem, Magic, and Ngspice.

The progress made thus far is learning how to utilize the tools to our given criteria, researching the ReRAM technology and how to implement it, and creating two new unique designs to go into our research chip. The client initially asked for four unique designs to be implemented in the open-sourced software to be then created into a research chip. Currently, we have four designs, two working designs from past groups and two in the design phase. We have learned to use the tools so our designs can be tested, fabricated, and placed on the project wrapper when they are prepared.

The plans for next semester consist of implementing our designs in the open-sourced software and testing each design to ensure that they are working properly. We also need to generate C-code to interface with the microcontroller in order to test which design is best for MVM within the ReRAM cells. If time allows, we will also be writing documentation to showcase how to interact with the microcontroller through C-code so future students can learn about ReRAM and the research chip.

Learning Summary

Development Standards & Practices Used

Below is a bulleted list of our circuit and hardware design practices. Also listed is the software that we are using to implement our designs and the engineering standards we have been following.

Circuit Design Practices:

- Analog and digital circuit integration
- Noise management
- Timing analysis
- Simulation and validation
- Device sizing and parameter optimization

Hardware Design Practices:

- Design for fabrication
- ReRAM-specific design considerations

Software Practices:

- Xschem (circuit design software)
- Magic (layout design software)
- Ngspice (simulation software)

Engineering standards:

- *IEEE 1481-2019- IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA)*: This is applicable to our project since it specifies how our integrated circuit should be examined using a variety of design automation tools for timing and power consumption.
- *IEEE 1076.4-2000- IEEE Standard VITAL ASIC Modeling Specification*: This standard is relevant to our project because it calls for the testing of an ASIC chip using extremely precise and effective simulation models.
- *IEEE 1149.4-2010- IEEE Standard for a Mixed-Signal Test Bus*: This is relevant to our project since it will have both digital and analog components, and we will need to properly test each one separately and in tandem.

- *IEEE 1364-2005- IEEE Standard for Verilog Hardware Description Language*: Since our project requires us to create Verilog code to facilitate communication between the wrapper and the analog portion, this standard is appropriate for us.

Summary of Requirements

- Four different ReRAM compute crossbar architectures must be present in the final tape-out.
- Component circuits are individually characterizable and accessible through analog pins.
- Uncertainty evaluation on architectures being implemented; the difference between simulated ideal crossbar current and actual within one ADC step.
- C Code for the MCU to interface with the ReRAM that enables testing and demonstrates that the ReRAM can compute an MVM within an epsilon tolerance.
- Bring up Documentation for FORMing the ReRAM Cells and characterizing the component circuitry via individual test benches.

Applicable Courses from Iowa State University Curriculum

- EE 330 - Integrated Electronics
- EE 465 - Digital VLSI Design
- EE 435 - Analog VLSI Circuit Design
- EE 501 - Analog and Mixed-Signal VLSI Circuit Design Techniques
- CPR E 281 - Digital Logic
- CPR E 288 - Embedded Systems I: Introduction
- CPR E 381 - Computer Organization and Assembly Level Programming

New Skills/Knowledge acquired that was not taught in courses

- ReRAM technology
- Open-source software: Xschem, Magic, Ngspice
- Skywater 130nm process
- Tape-out process of silicon chips

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Definitions

ReRAM: Resistive Random Access Memory

1T1R: ReRAM cell consisting of 1 transistor and 1 memristor

ADC: Analog to Digital Converter

XSchem: Open-source schematic creation software

Magic: Open-source layout creation software
Ngspice: Open-source analog simulation software
Gaw: Open-source analog waveform viewer

1. Introduction

1.1 Problem Statement

Matrix-vector multiplication (MVM) is one of the most common operations in machine learning applications. Performing MVM requires many multiply and accumulate operations, which takes a lot of time and energy in a typical CPU. Moving the required data back and forth in between the CPU and memory consumes a lot of energy in a traditional system. Compute-in-memory (CIM) technologies pose a potential solution to speeding up these processes by eliminating the memory bottleneck and allowing for parallel computation. ReRAM is an emerging, low-power, and non-volatile memory technology which may be used for CIM. Using ReRAM for CIM may require a rethink of ReRAM architectures. First, there is significant potential for impact from noise, both from the internal architecture of the ReRAM matrix as well as device noise from other chip components. Second, there are limited opportunities for ReRAM chip fabrication. For these reasons, we will design a fabricated test chip for ReRAM architecture exploration and characterization. The test chip will include multiple distinct ReRAM implementations in one design, resulting in a final chip that can test multiple implementations for research purposes. Ultimately, the test chip will be fabricated using the Skywater 130nm process and Efabless tools to give ourselves the best chance of getting a physical tape out.

1.2 Users and User Needs

The ISU ECpE faculty and their research teams (grad and undergrad) serve as the main client(s)/user(s) for this project. Secondary users include ChipForge, an Iowa State University club, while tertiary users encompass researchers and enthusiasts outside of our department. The objective of our project is to create a research test chip with multiple ReRAM architectures from past teams, in addition to our own, on the chip. In conjunction with the design of these architectures, comprehensive documentation will be produced to guide users on tool utilization, troubleshooting, and the design process. ISU research faculty will then use the chip to evaluate and characterize the different ReRAM architectures. Meeting the tapeout date with the final design will result in successful fabrication of the research chip which will meet the user needs. Additionally, in-depth documentation for the bring-up and testing will be necessary for the research teams to start evaluating the included architecture. To perform sufficient testing on each architecture, the research teams must be able to test and characterize each component individually to verify the functionality of system subcomponents. Along with testbench results, C code must be provided to allow the MCU to interface with the chip, performing testing and measurements.

1.3 What is ReRAM?

ReRAM is a part of emerging nonvolatile technologies that is aiming to address the limitations of conventional memory systems. ReRAM operates as a resistive switching, where a voltage induces a filament to grow between two electrodes. When the resistive material creates a filament it provides low resistance which entails a one. If the filament is broken then the resistance is high which creates a zero. There are three distinct modes for ReRAM; forming, writing and reading. Forming is when voltage is first applied to the cell to create the initial oxygen filament. Writing is where the filament is changed by the application of the electric field. Lastly, reading is where the resistance of the cell is transformed into binary data.

2. Requirements, Constraints, and Standards

2.1 Requirements

- Functional Requirements
    - Four different ReRAM compute crossbar architectures must be present in the final tapeout
        - Two architectures will come from the previous two team's final designs.
            - Both read from the bit line, and the source and word lines are parallel in both designs.
            - One utilizes a 4-bit ADC, while the other utilizes a 1-bit ADC
        - Two additional architectures will be newly designed by our team
            - One will be a true crossbar design, with no transistors; a matrix of memristors
            - One will parallelize the source and bit lines
    - Component circuits are individually characterizable and accessible through analog pins, and include the following:
        - One, three, and four bit ADCs
        - Transimpedance amplifier
        - ReRAM cell(s)
        - One, three, and four bit DACs
- Resource Requirements
    - Uncertainty evaluation on architectures being implemented; difference between simulated ideal crossbar current and actual within one ADC step
    - C Code for the MCU to interface with the ReRAM that enables testing and demonstrates that the ReRAM can compute a MVM within an epsilon tolerance
    - Bring-up Documentation for FORMing the ReRAM Cells and characterizing the component circuitry via individual testbenches.

2.2 Constraints

- Must use Efabless open source tools for design process
- Final design must pass pre check and tapeout check on Efabless servers before tapeout date on April 21, 2025

2.3 IEEE Standards

- *IEEE 1481-2019- IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA)*: This is applicable to our project since it specifies how our integrated circuit should be examined using a variety of design automation tools for timing and power consumption.
- *IEEE 1076.4-2000- IEEE Standard VITAL ASIC Modeling Specification*: This standard is relevant to our project because it calls for the testing of an ASIC chip using extremely precise and effective simulation models.

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- *IEEE 1364-2005- IEEE Standard for Verilog Hardware Description Language*: Since our project requires us to create Verilog code to facilitate communication between the wrapper and the analog portion, this standard is appropriate for us.

2.4 Applicable Courses From ISU Curriculum

- EE 330
- ENGL 314
- EE 230
- EE 465
- EE 435
- CPR E 381
- CPR E 288

3. Project Plan

3.1 Project Management/Tracking Procedures

We plan on using the agile methodology for managing our project. Since we meet with our advisors every week, we will do one-week sprints where we can give updates on what was accomplished in the past week. We will use GitHub issues to track tasks on our project. We will also be very deliberate when deciding to commit our changes, ensuring that any time we have our project in a state that we want to save or talk about we can look at the corresponding commit.

3.2 Task Decomposition

Task 1: Figure out the tools and research ReRAM functionality

- Installing toolchain
- Demonstrate competency with tools and refine ChipForge tutorials
- Get an analog device through Pre-check

Task 2: Verify and integrate previous architectures and peripheral circuitry

- Looking at other team's components and testing if they work
- Get the other team's components through pre-check

Task 3: Research and implement new architures

- Create schematic for new architecture #1
- Create schematic for new architecture #2
- Integrate new architectures into top-level design

Task 4: Create Final Layout of Design

- Create layout of circuit component testbench
- Add each unique architecture to the layout

- Clear all DRC Errors from the design
- Make sure the design passes LVS

Task 5: Verify Behavior of Final Design

- Perform post extraction simulation on components
- Perform post extraction simulation on unique architectures
- Verify that simulation results match expected behavior

Task 6: Get Final Design Through Efabless Checks

- Get final design through Efabless hosted precheck
- Get final design through Efabless hosted tapeout check

Task 7: Create Bring-up Documentation and C Code

- Write bring-up documentation
- Write accompanying C code for the project

3.3 Project Proposed Milestones, Metrics, and Evaluation Criteria

- All of the previous team's modules function as expected
- Post-integration of the previous team's modules function as expected while passing DRC and LVS checks
- We have created our own architectures that function as expected and pass DRC and LVS checks
- All four architectures are integrated and pass DRC, LVS, and precheck
- The parallel component circuitry has been integrated and passes DRC, LVS, and precheck

3.4 Project Timeline/Schedule

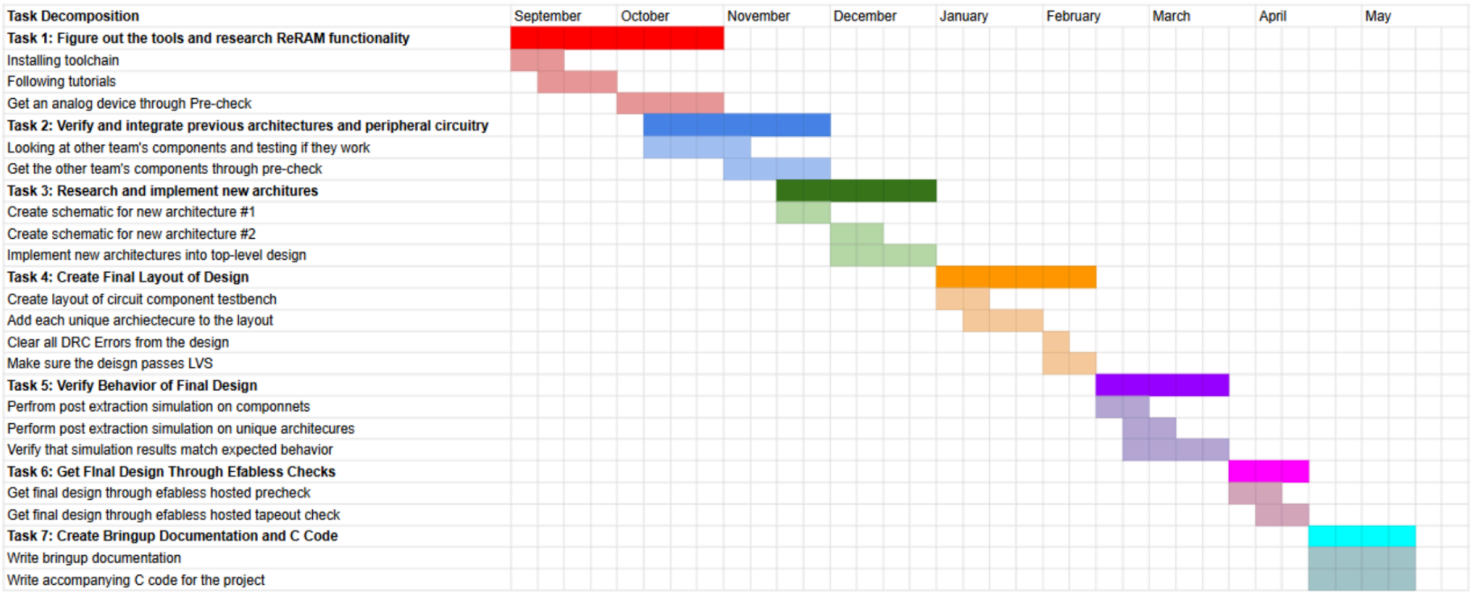

Figure 3.1: Gantt chart

3.5 Risks and Risk Management/Mitigation

- **Past team's design does not pass functional tests or pre-check**
    - **Risk 40% :** Past team's design does not pass functional tests or pre-check. Efabless tools have evolved over time, so past designs may no longer pass verification. Models may have been updated or files may be missing. To prevent a roadblock, we will begin by testing each component individually before integrating any of the designs to catch any problems early on. We may need to re-layout these components if they fail.
- **At least one of the new designs does not satisfy the requirements**
    - **Risk 15% :** There is a lot of potential for noise to interfere with the functionality of our circuits, as well as other various issues that could arise from our component circuitry. To mitigate this, we will make sure to do our research on different design architectures to produce a different process that our clients and end users will benefit from.
- **Integrated top-level project wrapper design fails functional tests or pre-check**
    - **Risk 65% :** Combining all of our components into one cohesive design may provide some issues while running the final checks. To mitigate this issue, we will make sure to run constant LVS and prechecks as we go along the integration process.
- **Flicker noise is more impactful on the Skywater process than expected**
    - **Risk 20%:** Finding the necessary values in the Skywater PDK to calculate the corner frequency between flicker noise and thermal noise has not been successful. In terms of simulation, there is not one agreed upon method of simulating flicker noise. Currently, we are unsure of what method our software is using, making simulation results more difficult to interpret. However, for most modern processes, the effects of thermal noise in the megahertz region are much more impactful than that of flicker noise [1]. Additionally, the impedance of the memristor will be much greater than that of any MOS device used in an architecture, so the dominant source of noise in these designs will be the ReRAM cells. To mitigate this potential risk, we can increase the clock speed of our circuit to around 20MHz where thermal noise will certainly be dominant.

3.6 Personnel Effort Requirements

	Time
Task 1: Figure out the tools and research ReRAM functionality	**70 hrs**
Installing toolchain	10 hrs
Demonstrate competency with tools and refine ChipForge tutorials	40 hrs
Get an analog device through Pre-check	20 hrs
Task 2: Verify and integrate previous architectures and peripheral circuitry	**120 hrs**
Looking at other team's components and testing if they work	60 hrs
Get the other team's components through pre-check	60 hrs
Task 3: Research and implement new architures	**90 hrs**
Create schematic for new architecture #1	30 hrs
Create schematic for new architecture #2	30 hrs
Integrate new architectures into top-level design	30 hrs
Task 4: Create Final Layout of Design	**50 hrs**
Create layout of circuit component testbench	20 hrs
Add each unique architecture to the layout	20 hrs
Clear all DRC Errors from the design	5 hrs
Make sure the design passes LVS	5 hrs
Task 5: Verify Behavior of Final Design	**80 hrs**
Perform post extraction simulation on components	20 hrs
Perform post extraction simulation on unique architectures	30 hrs
Verify that simulation results match	30 hrs

expected behavior	
Task 6: Get Final Design Through Efabless Checks	**60 hrs**
Get final design through Efabless hosted precheck	30 hrs
Get final design through efabless hosted tapeout check	30 hrs
Task 7: Create Bring-up Documentation and C Code	**40 hrs**
Write bring-up documentation	20 hrs
Write accompanying C code for the project	20 hrs

Table 3.1: Personnel effort requirements

3.7 Other Resource Requirements

All of the CAD tools are open-source software. However, the software that will be used is not well documented so we have to rely heavily on previous teams documentation and tutorials. The other resources are used to create schematics and layouts and test the functionality of the components and circuits. These resources include:

- Xschem: Schematic capture
- Magic: Layout
- Netgen: LVS
- Slack: online community for help with open source toolset

We also have access to the lab in Durham 310, which has FPGAs that we can use through their comparch computer. We may need to design a PCB breakout board once our design is fabricated, for which we can use ChipForge documentation. Finally, we have $9,750 for the ReRAM Efabless tapeout for ChipIgnite 2504, which is provided to us by our client, Dr. Duwe, through an NSF award.

4. Design

4.1 Broader Context

4.1.1 Broader context

The test chip is designed for the research and engineering community. This chip will explore the next-generation of in compute memory. The communities that are being affected by this design are data-intensive industries such as healthcare, finance, autonomous systems, and machine learning will benefit from the reduced energy consumption associated with ReRAM compute in memory systems. Lastly, the societal needs that our project addresses are energy efficiencies and technological advancement which create competitiveness in the future for technology.

Area	Description	Examples
Public Health, Safety, and Welfare	The ReRAM test chip will demonstrate computational efficiency potentially reducing energy consumption of artificial intelligence machine learning. This can benefit communities by lowering energy demand and associated emissions	Reducing energy consumption would decrease greenhouse gas emissions which will improve the quality of the air in areas with significant computational infrastructure.
Global, Cultural, and Social	By advancing energy-efficient technology, this project aligns with the global efforts towards sustainable and energy reductions, valued by diverse and professional communities.	The project supports globe sustainability initiatives by reducing the carbon footprint of computational operations.
Environmental	ReRAM aims to reduce energy consumption and create low powered technologies compared to traditional memory. However, the fabrication process might use hazardous material, so that effect is unknown.	While the energy usage during the operation of the ReRAM compute-in-memory systems is reduced. The manufacturing process of the ReRAM cells, such as transition metal oxide, must be evaluated to ensure sustainability.
Economic	The cost of this device may be expensive at first but it creates a more energy efficient outcome. In the long run it will make	Successful implementations of ReRAM compute-in-memory systems will create job opportunities in low-power hardware design and manufacturing.

Table 4.1: Broader context

4.1.2 Prior Work/Solutions

Since ReRAM is an emerging technology, especially for compute purposes, there are no commercially available solutions on the market. We have looked closely, of course, at the previous two senior design team's projects for reference. In addition, the ISAAC design is an example of an academic implementation of a ReRAM-based true machine learning accelerator. The table below lists pros and cons of each of these designs, as well as our design.

Product	**Pros**	**Cons**
ISAAC ReRAM-based CNN Accelerator [3]	• Acts as a true AI accelerator • Uses 1T1R grid for more precise memristor writes • Shared ADC allows for better precision	• Shared ADC requires sample and hold circuits • Very specialized to one application, not as general for research
Design made by sddec23-08	• Uses 1T1R grid for more precise memristor writes • Multiple ADCs; one for each read line	• Multiple ADCs = less precision (1 bit) • Only includes one ReRAM architecture
Design made by sddec24-13	• Uses 1T1R grid for more precise memristor writes • Shared ADC allows for better precision	• Shared ADC requires sample and hold circuits • Only includes one ReRAM architecture
Our design	• Includes four individually accessible unique ReRAM architectures • Includes individually characterizable component circuitry • Generalized for research purposes	• Research-focused, unlikely to be useful in a true machine learning context • Could suffer from over-complication since it includes many different designs

Table 4.2: Pros/Cons of prior work/solutions

4.1.3 Technical Complexity

Our design presents a variety of technical challenges:

1. Since we are using open source software, none of our team members are familiar with the tools we are using. This provides a barrier of entry to getting started with our actual design.
2. ReRAM is an emerging technology, and there are very few opportunities available for fabrication of ReRAM chips. Also, there is little information about ReRAM usage for compute-in-memory applications, so we are exploring a new frontier.
3. We are including four different ReRAM architectures in our design, which of course increases the complexity of our design. However, this will likely help us down the line: if we find that one of our architectures doesn't work as intended, there are still three others to test.
4. We are also integrating a number of components acting as the peripheral circuitry of the design. This includes S&H circuits, TIAs, DACs, and ADCs. While our team doesnt have direct experience with each of these components, they are very well studied in academia and in industry, so finding documentation about them shouldn't be a struggle.

4.2 Design Exploration

4.2.1 Design Decisions

1. New ReRAM Architectures
2. ADC Resolution
3. Drive voltages for different operations: FORM, write, read, compute
4. Taking outputs from the source line or bit line

4.2.2 Ideation

One of the key uncertainties in our design process is whether we will be able to achieve precise and accurate data retrieval from the output line. Currently, we are still in the process of determining the length of the interconnects and assessing the level of noise that must be accounted for when acquiring data from the output. This is why the selection of an appropriately designed Analog-to-Digital Converter (ADC) is critical to the success of the project. The ADC choice will not only determine whether the project is feasible but will also play a crucial role in ensuring the functionality and scalability of the system in the broader context of the project. This includes the goal of enhancing the performance of AI accelerators by reducing power consumption and improving processing speed.

Additionally, we are reviewing the designs developed by our previous team, with the possibility of incorporating elements of their architecture into our own designs. Their work includes the use of a 4-bit Flash ADC and a Sample-and-Hold (S&H) ADC, both of which provide useful insights and potential integration points for our architectures. Below are five potential ADC design approaches that we are considering in our two architectures.

- Current_Mode ADC

- 4-bit Flash ADC
- 1-bit S&H ADC
- Delta Sigma ADC
- Pipeline ADC

4.2.3 Decision-Making and Trade-off

Below is a table that weighs the benefits and drawbacks of each ADC design. With the use of this table and previous designs, we will choose whether we want to implement a new ADC within our designs that differentiates from the previous teams or utilize one of theirs.

Architecture Type	Pros	Cons
Current-Mode ADC	It can handle small variations in current levels and use low power consumption.	Susceptible to small amounts of noise and low resolution compared to other ADC designs.
4-bit Flash ADC	Fast conversions as well as simplicity in design with ideal parallel processing.	High power consumption as well as large area and susceptible to noise environments.
1-bit sample and hold ADC	Extremely fast conversions, extremely low power consumption, and simplicity in design.	Only limited to binary decision-making, not suitable for high precision applications, and sensitive to noise.
Delta Sigma ADC	Very high resolution with exceptional precision and accuracy. Great noise reduction.	Very slow and has higher power consumption compared to other ADC designs.
Pipeline ADC	High speed with fast conversion rates, making it useful for high-speed applications.	More complex than other ADC designs and has high power consumption. It may lack high resolution based on the application.

Table 4.3: Comparing ADC architectures

4.3 Proposed Design

4.3.1 Overview

Our design aims to characterize four unique matrix-vector multiplication modules that utilize ReRAM for performing compute-in-memory operations. These modules will consist of component circuitry, the first of which is the ReRAM crossbar itself. The ReRAM crossbar is a matrix of ReRAM cells where the actual computation will take place. Another component circuit is the trans-impedance amplifier (TIA), which will convert currents into voltages which will represent the result of the operation. The final major component circuit is the ADC, which will convert our analog result into a digital value readable by the CPU. Each component circuit will be individually characterizable as part of our design as well.

4.3.2 Detailed Design and Visuals

The goal of this design is to combine four different ReRAM crossbar architectures into one top-level block design. These will all be connected to the microcontroller via Logic Analyzer Pins, which are responsible for communication between the microcontroller and the ReRAM crossbar systems, such as reading values from the current crossbar or sending values to it. Two of the ReRAM crossbars will be sourced from the previous teams' designs, while the other two will be original designs. The original designs should closely resemble the previous designs, with minor architectural changes, such as swapping the directions of the source and bit lines. The top-level design should also include separate, individually characterizable testbenches for the different types of peripheral circuitry, including the ADC, DAC, and TIA. The top-level diagram outlines the design, while a lower diagram presents a potential internal design for a ReRAM crossbar. The ReRAM crossbar consists of a matrix of ReRAM cells connected by lines called bit lines, source lines, and word lines. The matrix is preloaded with values by setting the conductances of each memristor in the matrix, and input values are sent into the matrix via either the bit line or the source line, depending on the specific architecture. The previous teams' designs should be used in depth as references when designing the new architectures.

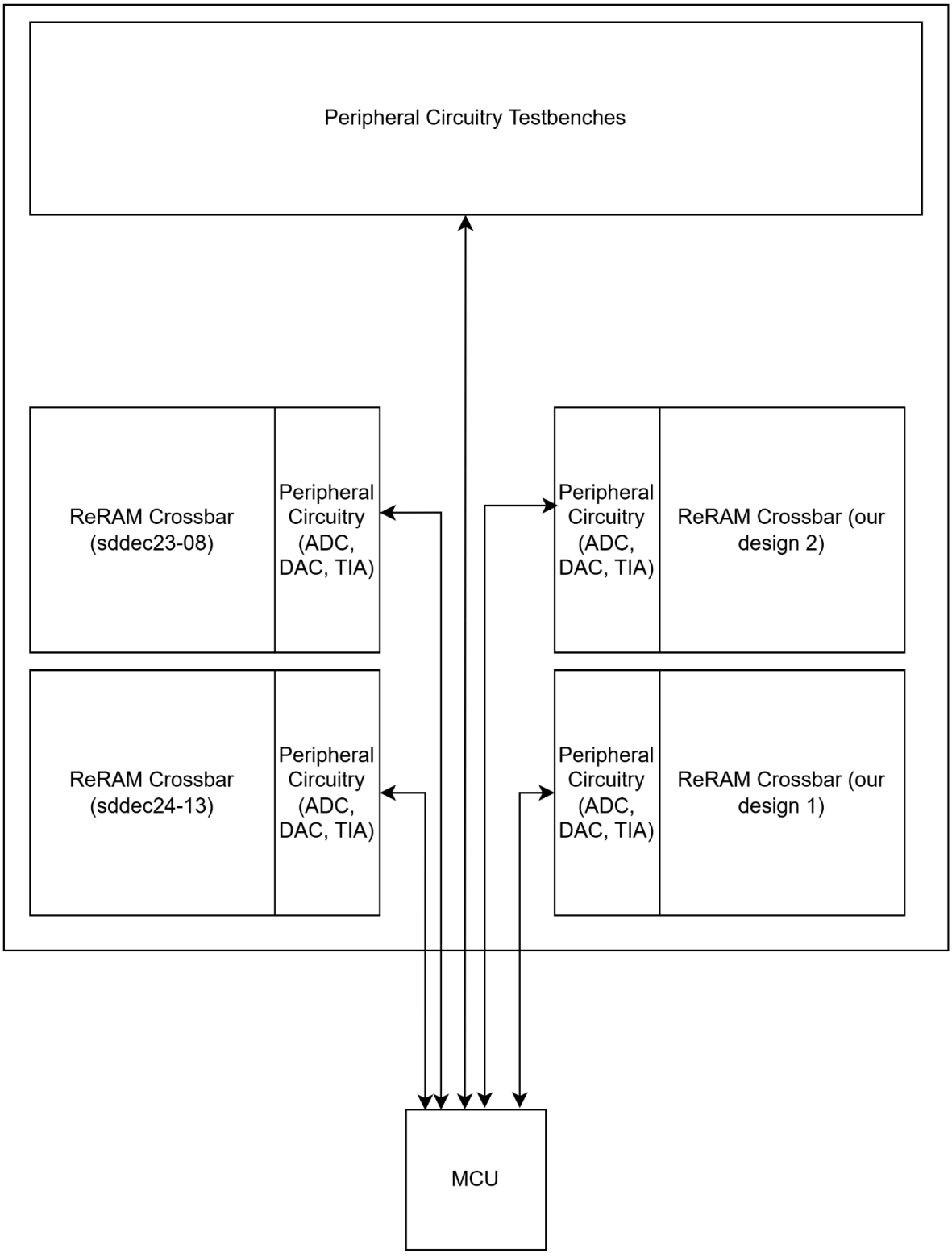

Figure 4.1: Top level block design

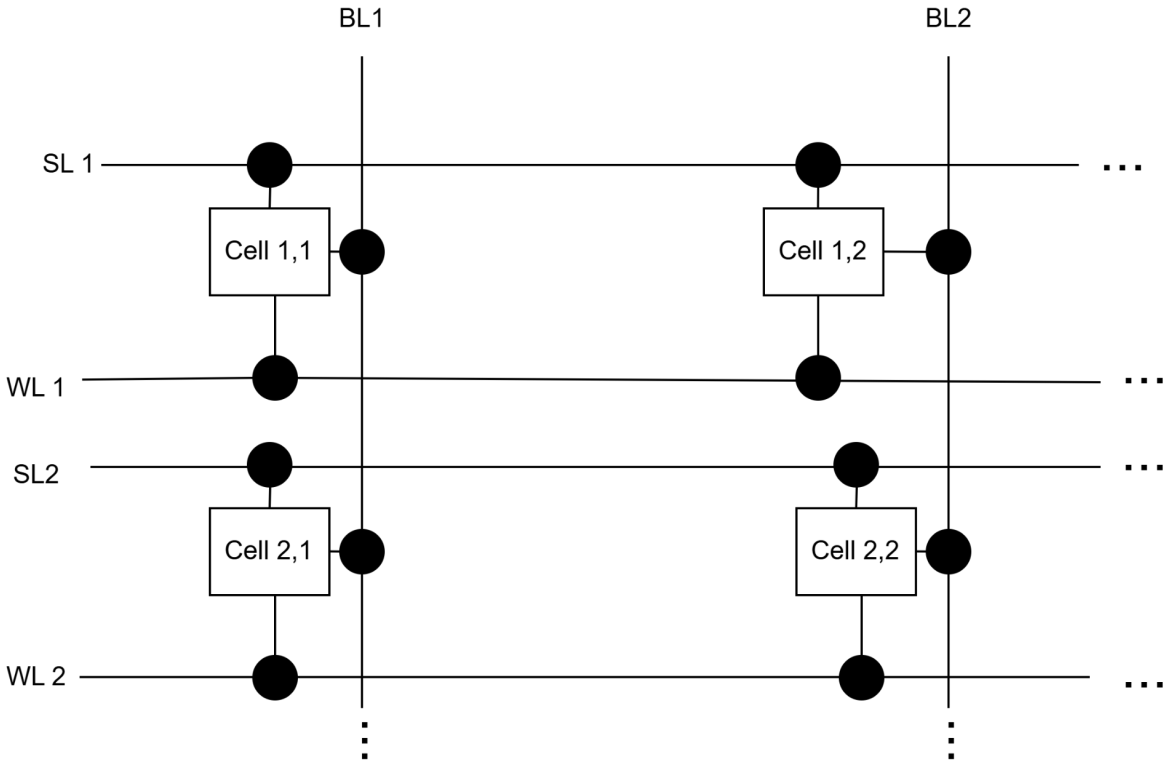

Figure 4.2: Schematic for one ReRAM crossbar architecture

4.3.3 Functionality

Once fabricated, our chip will act as a daughter board that can be connected to a microcontroller. The microcontroller will perform FORMing operations to set up the ReRAM cells for computation. The microcontroller will also be able to send and receive data from each architecture on the chip, in addition to the peripheral circuitry testbench. During read/write operations to the chip, the microcontroller will be able to perform multiply and accumulate operations on each architecture. This data, in combination with characterizations performed in the peripheral circuitry testbench will allow the users to characterize the components and also get a better understanding of which ReRAM architectures are better suited for compute in memory workloads.

4.3.4 Areas of Concern and Development

Our design plan currently meets our user requirements by containing four unique ReRAM crossbar architectures and individually characterizable component circuitry. Our biggest concern moving forward with our design will be about the feasibility of our ReRAM crossbar architecture designs. As we complete simulations, we may find that certain configurations of ReRAM cells don't effectively carry out the operations necessary for our design to meet requirements. If this is the case, we will need to either change the configuration of the faulty architecture or come to a conclusion backed by concrete evidence that four unique adequate architectures do not exist.

4.4 Technology Considerations

Our design presents a variety of technical challenges:

1. Since we are using open source software, none of our team members are familiar with the tools we are using. This provides a barrier of entry to getting started with our actual design.
2. ReRAM is an emerging technology, and there are very few opportunities available for fabrication of ReRAM chips. Also, there is little information about ReRAM usage for compute-in-memory applications, so we are exploring a new frontier.
3. We are including four different ReRAM architectures in our design, which of course increases the complexity of our design. However, this will likely help us down the line: if we find that one of our architectures doesn't work as intended, there are still three others to test.
4. We are also integrating a number of components acting as the peripheral circuitry of the design. This includes S&H circuits, TIAs, DACs, and ADCs. While our team doesnt have direct experience with each of these components, they are very well studied in academia and in industry, so finding documentation about them shouldn't be a struggle.

4.5 Design Analysis

Although we haven't implemented or tested anything regarding our final integration and architectures, we have decided on the designs of our two unique architectures. In terms of implementation, we have designed an original testbench for a 1T1R cell to test the behavior of individual ReRAM cells. We have also designed an inverter module that has been taken all the way through the testing and integration process. This gave us a very simplified version of the design, integration, and test process that we will have to follow throughout our project, building our knowledge and expertise with the tools and methods we will use to carry out the ReRAM project. Currently, we've been testing the modules that the first team designed, ensuring that they function as intended and are reliable when we integrate them into our final design. Though we haven't been able to run into any issues regarding our final design due to us not implementing or testing it yet, we are taking precautions to minimize any major issues that we may run into. We'll be sure to run precheck tests early and often, making sure that any significant progress toward a final design will be thoroughly tested and integrated, preventing an overwhelming debug during the final stretch of our project.

5. Testing

The nature of our project requires rigorous testing, as there are many different components that all must work separately and also must be integrated together in order to reach our final product. Each component circuit, whether inherited from previous group's designs or newly designed by our group, must have an individual testbench that works as expected. In addition, these components must remain functional when integrated together. To ensure that there are no unexpected issues, our team's testing philosophy will be to continuously test and integrate new components and run our design through pre-check each time we make changes. This ensures that we never add too many features at one time, so that if issues arise we can solve them swiftly by identifying the most recent change.

5.1 Unit Testing

Every individual component circuit must be tested. For each circuit, we will need to create a schematic testbench using XSchem that we can use to characterize the behavior of our circuit and compare it to expected behavior. This testbench can also be used for post-layout simulation, which will need to be carried out for each component circuit as well. The layout process, which we will perform using Magic, introduces parasitics that need to be simulated post-layout. Magic also includes tools for extracting SPICE netlists from our layouts. Whether simulating pre-layout or post-layout, we will use Ngspice to carry out our simulations and Gaw for viewing our resulting waveforms. For the ReRAM compute architectures, each individual cell will need to be tested. Our component circuitry will also need testbenches created. All of these individual testbenches will be included in our final top-level design, so that we can characterize our component circuitry post tapeout.

5.2 Interface Testing

There are two main interfaces in our design, one between the individual components within our ReRAM architectures and one between all of our analog circuitry and the on-chip RISC-V processor. Within our ReRAM architectures, we will need to connect our component circuitry to the appropriate lines in our crossbar, which depends on the unique architecture. This will be tested iteratively. Using XSchem for testbenches, Magic for layouts, Ngspice for simulations and Gaw for waveform viewing, we will combine component circuits one at a time and test each time a component is added. Using this strategy, we will be able to determine what component is acting out of accordance with our expectations and make adjustments to our design as needed.

For the interface between our circuitry and the processor, we will need to integrate our full design into the Efabless-provided analog wrapper. This is where we can make all of our connections to the logic analyzer pins, which can then be directly interfaced with via the processor.

5.3 Integration Testing

The most critical integration path in our design will be the integration of our analog circuitry into the analog wrapper circuit that allows for communication between the RISC-V processor and our circuitry via logic analyzer pins. Per the requirements of our project, our four

ReRAM architectures must be accessible via logic analyzer pins, as well as individual component testbenches for characterization and testing purposes. To test this integration, we must first test our high-level analog circuitry as an entire unit to ensure that it is working properly using the same methods mentioned in the above sections. Once these tests are completed, we can then move on to integrating the high-level analog circuitry into the analog wrapper, which consists of connecting the appropriate logic analyzer pins to the inputs and outputs of our circuit.

5.4 System Testing

Once our circuit is complete and integrated into the analog wrapper, it will be time to create test cases for testing the functionality of our design. We will develop C code that performs the multiplication using each of our four ReRAM architectures and test that our processor can dispatch these operations to our analog circuitry and receive output back from our circuit. We also must develop C code for testing our individual component circuits. By using C programs, we will test the entire system, which includes the interface between the processor and our analog circuitry.

5.5 Regression Testing

On a project like ours, regression testing is critical to a smooth development process. Our action plan for regression testing involves integrating only one component at a time, and passing pre-check each time something new is added. This ensures that we can solve pre-check issues with individual components as we go, which is better than adding all the components together and then trying to run pre-check. If we tried the latter option, we would likely have trouble quickly determining which component was causing the problem, delaying progress on our project.

5.6 Acceptance Testing

Firstly, in order for our design to be accepted, it must contain all the components mentioned in our requirements. This includes four ReRAM architectures with accompanying component circuitry, as well as individually characterizable component circuit testbenches. If these are present in the design, then we will move on to the second acceptance criteria.

Second, our design must pass the Efabless-provided pre-check and tapeout check on the Efabless servers by the tapeout date, which is Apr 21, 2024. If our design passes all checks and contains all required components, it will be acceptable.

5.7 Security Testing

Security testing is not applicable to our design.

5.8 Results

For a lot of the semester, we were focused on gaining familiarity with the open source tools. In order to accomplish this, we chose to design an inverter, run simulations on our inverter, create a layout, integrate it into the analog wrapper, and run through pre-check. Running through the whole process with a simple component circuit like an inverter helped us learn the toolchain and exposed us to some common issues that we can work through. This process showed us that the tools are often frustrating to use and there are many different problems that can arise while

going through the design process. However, moving forward, we are now better equipped to take on errors that occur when working with the tools.

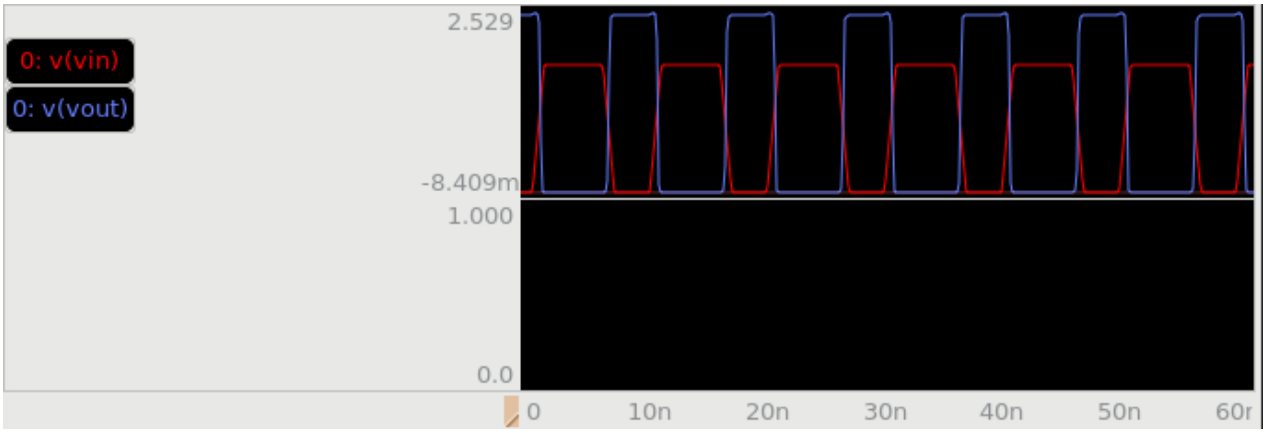

Figure 5.1: Simulation results from inverter, pre-layout

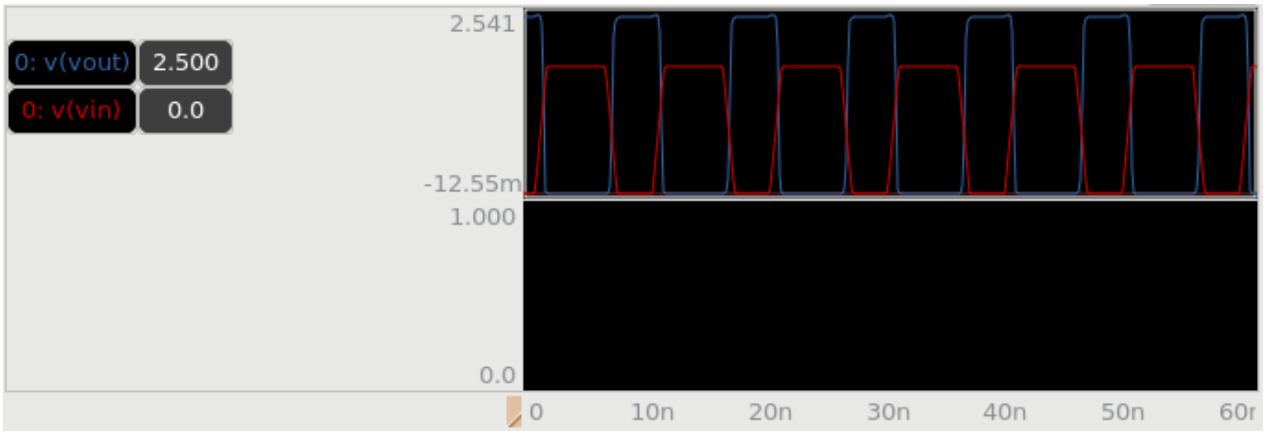

Figure 5.2: Simulation results from inverter, post-layout

When exploring potential design decisions for our unique architectures, we considered the idea of using PMOS transistors instead of NMOS transistors. The previous two design teams both used NMOS transistors. In order to explore this idea further, we designed a testbench which compared two ReRAM cells, one using a PMOS transistor and the other using an NMOS transistor. The poor results of this test, along with our own research and assistance from faculty advisors, caused us to shift our focus to other potential design decisions. Despite the suboptimal results, this was still a design decision worth discussing.

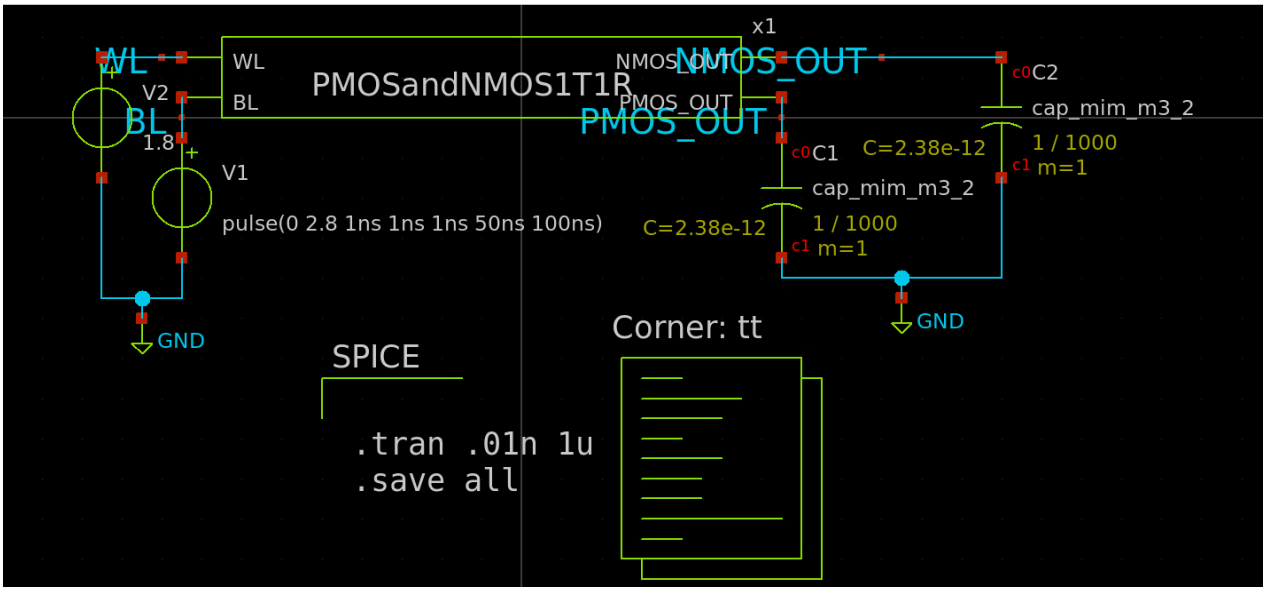

Figure 5.3: Testbench for comparing 1T1R cells using PMOS and NMOS transistors

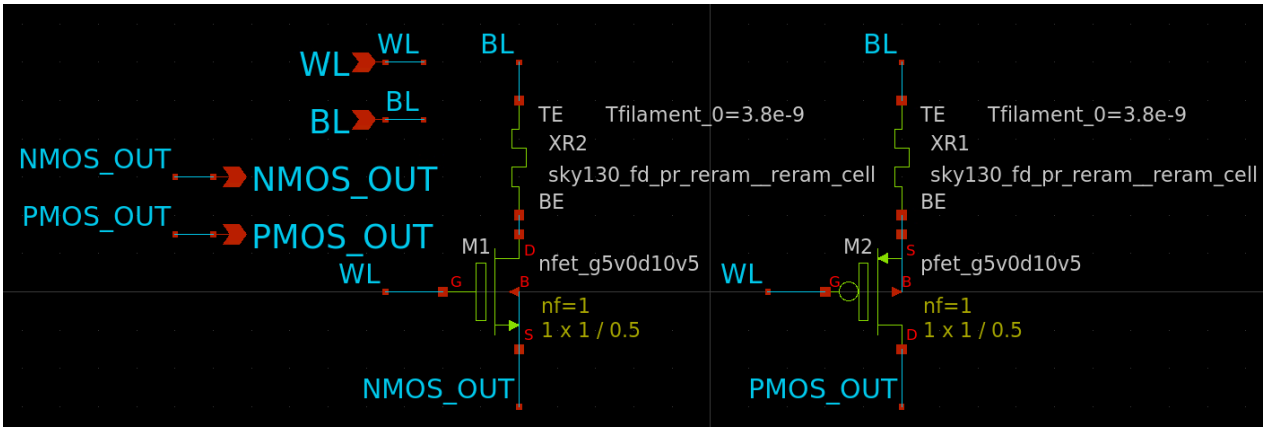

Figure 5.4: Schematic including two 1T1R cells, one using a PMOS transistor and the other using an NMOS transistor

We have many testing results from the sddec23-08 design team's testbenches. Testing these components helped us gain more familiarity with Ngspice and Gaw waveform viewer. It also gave us an opportunity to see what components from the previous team we could utilize in our design, what components we could modify to fit our design, and what components we may need to revamp for our use.

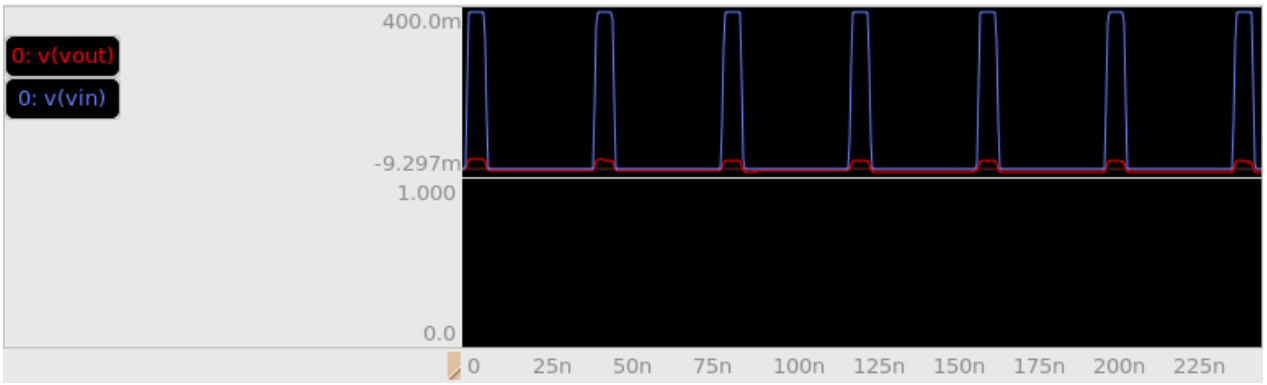

Figure 5.5: Resulting waveforms from buffer testbench from team sddec23-08

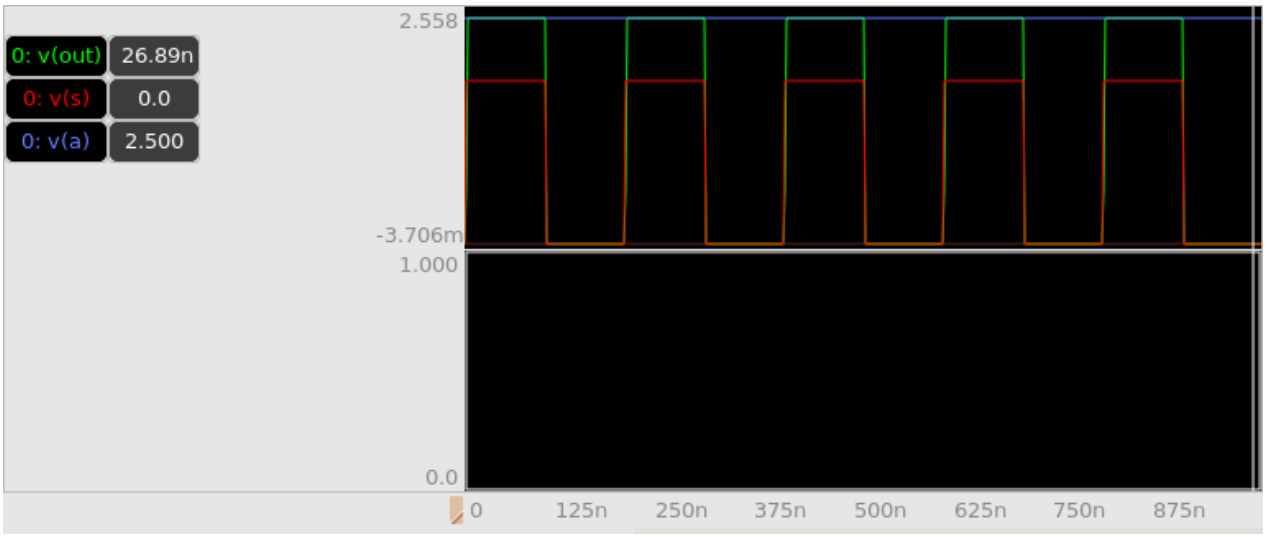

Figure 5.6: Resulting waveforms from 2-to-1 multiplexer testbench from team sddec23-08

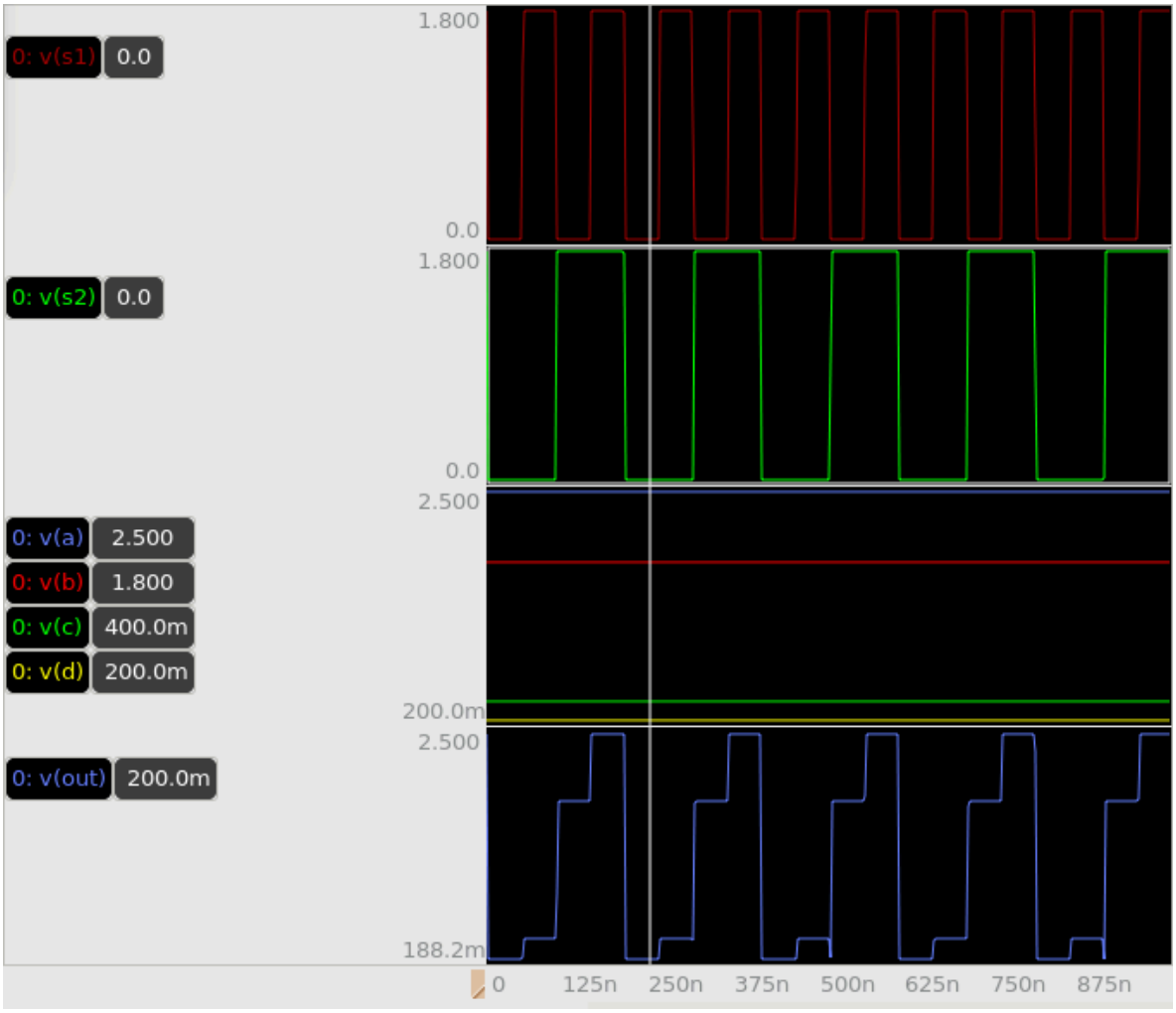

Figure 5.7: Resulting waveforms from 4-to-1 multiplexer testbench from team sddec23-08

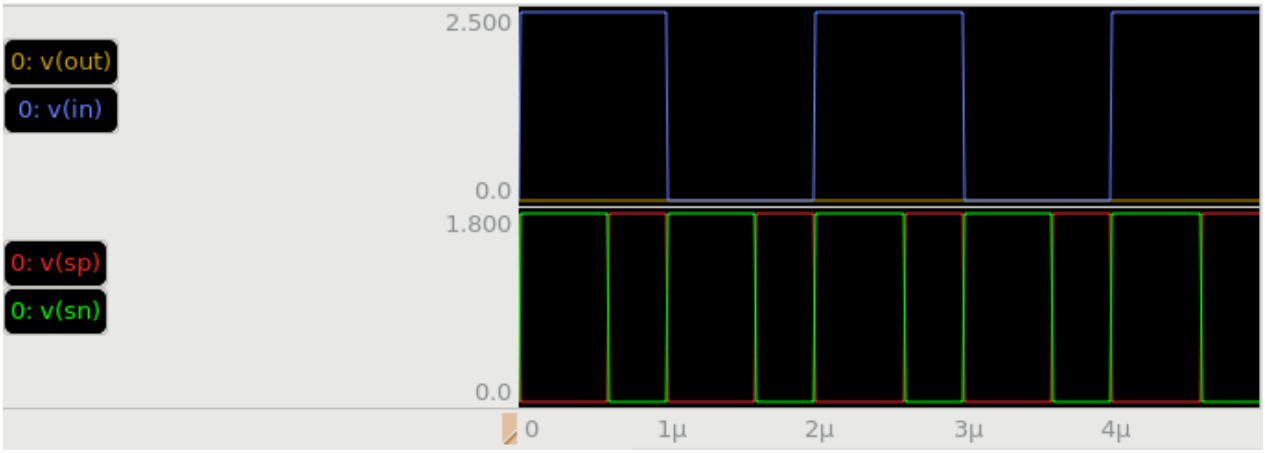

Figure 5.8: Resulting waveforms from transmission gate testbench from team sddec23-08

The schematic below shows our work to test and characterize a pre-layout 1T1R cell in xschem. Since moving away from the idea of using a cell with a PMOS device, the testbench below only includes a NMOS device for testing purposes. In order to read the value of the ReRAM, the MOS device is kept in the triode region. Seen on vsource component (V2) the input signal is a ramp function that increases from 0V to 2.5V and then decreases from 2.5V to -2.5V before finally settling back at zero. This input signal should demonstrate the SET and RESET states of the device. We measure the state of the device by observing drain-source voltage and drain current of the transistor while comparing them to the input waveform.

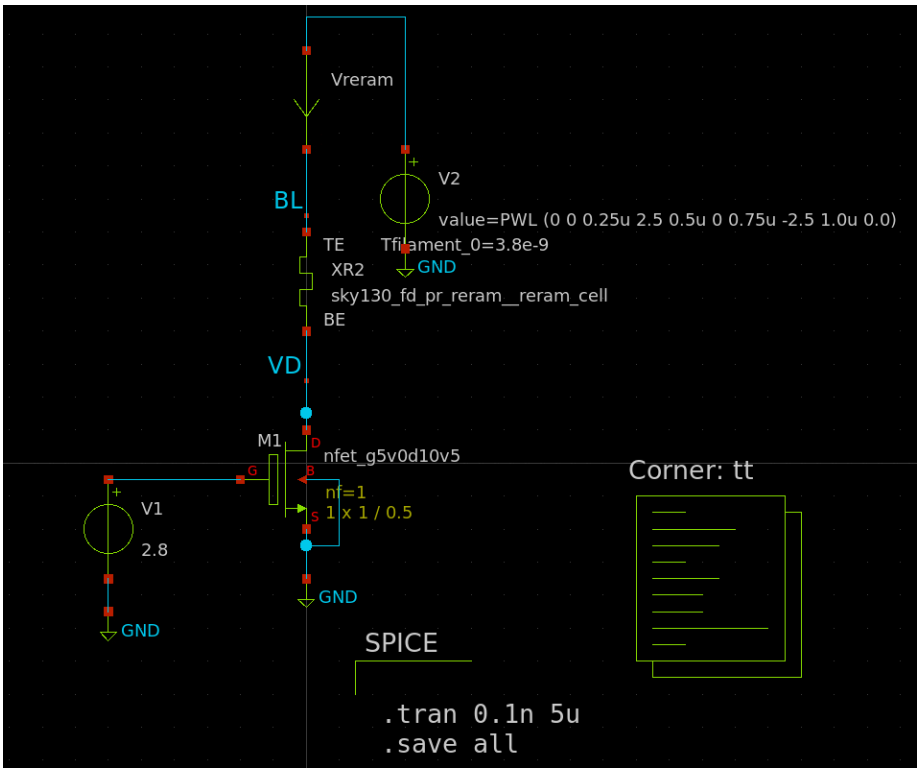

Figure 5.9: 1T1R testbench

The waveforms below represent the successful SET and RESET operations of the ReRAM cell in the testbench above. The ReRAM cell enters the SET state as i(vreram) begins to peak. When ReRAM enters the SET state, it transitions to a high conductance material, which we can see in increase in current conducted through the transistor. In order to transition the ReRAM cell to the RESET state, a negative potential needs to be applied across the cell. As the negative potential is applied, the ReRAM cell will transition back to the low conductance state. We can see this transition to the RESET state in the waveform below around 600ns where the current drops to near zero when a sufficient negative potential is applied across the cell.

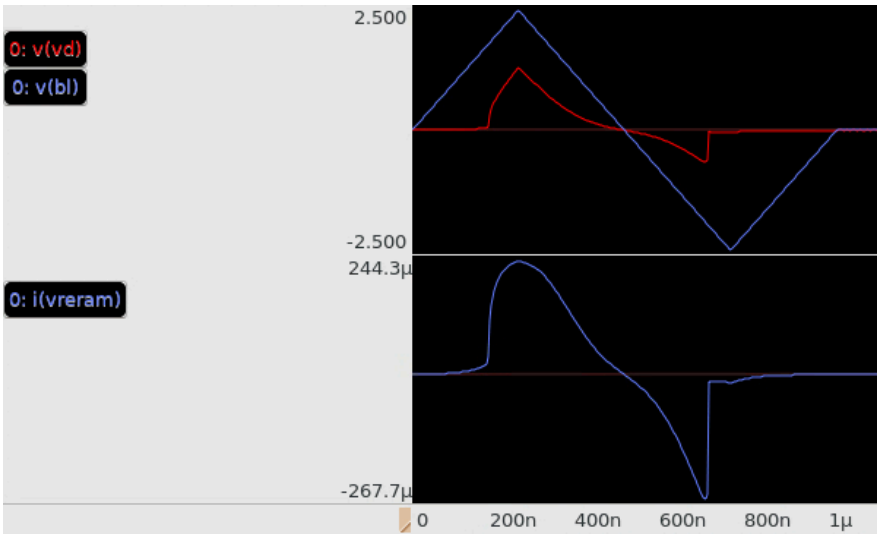

Figure 5.10: Waveforms from our 1T1R testbench

6. Implementation

Thus far, the implementation process has focused on testing and verifying inherited components from previous teams while integrating newly designed elements. Key achievements include developing unit testbenches for individual components, such as MUXs and transmission gates, and verifying their behavior using the simulation tools Ngspice. Additionally, a comparative analysis was conducted on PMOS- and NMOS-based ReRAM cells using a custom testbench. The results of this analysis informed the selection of transistor types for new architectures shall remain NMOS, as mentioned in section 5.8.

Visual representations, including testbench schematics and simulation results, have been instrumental in guiding the implementation process. Key visuals include schematics comparing PMOS and NMOS testing, pre-layout and post-layout simulation results for constructed circuits, and waveform outputs from inherited designs like buffers and multiplexers. These efforts build upon previous work while ensuring robust and reliable implementation of new designs.

We are implementing two new ReRAM architectures. One will parallelize the source and bit lines. The design for this architecture can be seen in Figure 6.1 [6]. In this design, the source and bit lines are arranged in parallel, which simplifies the routing of signals. This setup can improve signal uniformity and reduce power loss caused by electrical resistance. However, placing the lines so close together increases the risk of coupling noise, where signals from one

line interfere with another. The goal of this design is to explore how noise can be managed in such a configuration while seeing if the benefits of simpler routing outweigh the drawbacks.

The other architecture will be a true crossbar design with no transistors, essentially being a matrix of memristors. The design for this architecture can be seen in Figure 6b [6]. This design removes transistors entirely, leaving only a matrix of interconnected ReRAM cells. Without transistors, the cells lack isolation during read and write operations, meaning all cells are connected at once. This can lead to issues like leakage currents, which waste power, and signal interference, where neighboring cells affect accuracy. On the other hand, removing transistors has key advantages. It makes each cell much smaller, maximizing the use of space. This also reduces manufacturing complexity and cost. Additionally, the fully connected structure is excellent for handling many calculations at the same time, which is perfect for compute-in-memory tasks. By testing this design, we hope to find ways to overcome its challenges while taking advantage of its simplicity and efficiency.

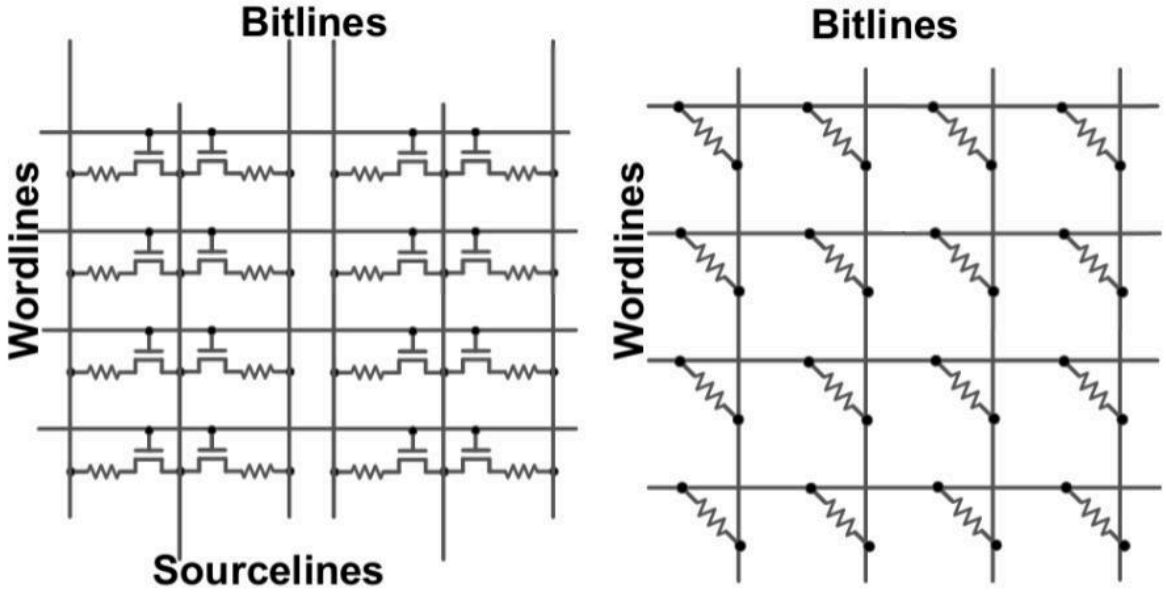

Figure 6.1: (a) Parallel Bitline and Sourcelines. (b) True Crossbar Design (both extracted directly from [6])

For the upcoming semester, we plan to build on the progress made this semester. With proper testing for each component, we will begin to use these modules to create our final top-level system. This includes implementing prior architectures, our newly designed architectures, and our peripheral circuitry. After this implementation, we will run a series of test cases to ensure the circuits function correctly before connecting to the harness. Finally, we will make any necessary adjustments to ensure the design passes the precheck and is successfully submitted through the Efabless program.

7. Ethics and Professional Responsibilities

Engineering ethics means following guidelines that are in the best interests of the client, the public, and the engineering profession. Adhering to these guidelines, this team seeks to ensure that the ReRAM-based architectures reduce energy consumption and improve computational efficiency for extensive tasks like machine learning. During the process, we are being mindful of being honest and transparent, and being accountable and responsible. Accessing the capabilities, risks, and limitations of ReRAM and providing documentation and testing results will provide the client with accurate data to make an honest decision about their product. Regarding the complexity and uniqueness of ReRAM, we will be proactive in addressing errors that arise during the project, and if we uncover any flaws in the ReRAM architecture, we will work quickly to correct them.

Professional responsibilities mean being held up to specific standards and duties that engineers have to their profession, colleagues, and the public. Thus, our project must amplify the integrity of research, collaboration of knowledge, and advocacy for fair and equitable access. We must ensure that the test chip is capable of producing valid results, which includes rigorous testing, validation, and documentation of our findings, which will help with the future development of the chip. As we explore and test ReRAM architectures, we must consider the long-term implications of this technology and aim to ensure that the benefits of our ReRAM findings will be accessible for further innovations and diverse industries.

7.1 Areas of Professional Responsibility/Codes of Ethics

The chosen code of ethics for the table below is the IEEE.

Area of Responsibility	**Definition**	**Relevant Items from the Code of Ethics**	**Team Interaction with the Code**
Work Competence	The ability of an engineer to perform their job when faced with challenges ensures that they are qualified by enhancing or maintaining their technical skills.	*"To maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience, or after full disclosure of pertinent limitations."*	Our team has actively sought knowledge through research papers, external consultations, and expert feedback from the open-source company. To stay up to date, we review current literature and continue to ask experts.
Financial Responsibility	Refers to the ethical obligation of engineers to manage financial resources wisely, transparently, and with integrity	*"To avoid unlawful conduct in professional activities, and to reject bribery in all its forms."*	Most of our tools are open-sourced. However, we have a tape-out date in April to produce one hundred chips for ten thousand dollars. We need to use our time responsibly in order to have a working and cost effective design.

Communication Honesty	Engineers should provide truthful and accurate information to avoid any misleading claims.	*"To seek, accept, and offer honest criticism of technical work, to acknowledge and correct errors."*	We maintain transparency when we encounter both successes and challenges we face. Any design changes are also openly discussed.
Health, Safety, Well-Being	Engineers will ensure the health, safety, and well-being of the public when creating designs and performing their work.	*"To hold paramount the safety, health, and welfare of the public, to protect the privacy of others, and to disclose promptly factors that might endanger the public or the environment."*	Our team runs regular risk assessments that may pose any safety hazards, especially with concerns about overheating and ReRAM material production.
Property Ownership	The ethical responsibility of engineers is to respect the intellectual property rights of others, including patents, copyrights, trademarks, and trade secrets.	*"To be honest and realistic in stating claims or estimates based on available data, and to credit the contributions of others properly."*	We foster a collaborative environment where any ideas are welcome and given credit.
Sustainability	Engineers should strive for environmentally friendly and stable designs that can be used in the long term.	*"To strive to comply with ethical design and sustainable development practices."*	By using ReRAM cells, we are decreasing the power consumption from the memory to the arithmetic logic unit back to the memory.
Social Responsibility	Engineers should create products and services that contribute to the well-being of the community and society, not to their own greed.	*"To improve the understanding by individuals and society of the capabilities and societal implications of conventional and emerging technologies, including intelligent systems."*	With the emerging ReRAM technology, we are also creating tutorials, and documentation that will help future innovators and the public to use for their own ideas and sound minds.

Table 7.1: Codes of ethics

To further contribute to the table above, the professional responsibility that we perform well in is work competence. Knowing little to no knowledge about the emerging ReRAM-based technology, we had to find research papers that were based on the infamous ReRAM cells and how to compute in memory matrix-vector multiplication. We have also consulted experts in various fields for noise minimization, very large circuit integration (VLSI), and tool usage.

One area of professional responsibility that requires improvement is financial responsibility. As previously mentioned in the table, we have a tape-out deadline in April, meaning that all our designs, schematics, layouts, and wrappers must be completed by then. The

client is relying on our design to produce one hundred chips, each costing one hundred dollars, so our project must undergo rigorous testing through open-source software to ensure the design functions as intended. We have faced challenges in creating a design that is distinct from previous teams' work. However, given the tight deadline and the significant financial investment involved, it is crucial that we choose a solid design that can be completed successfully within the available time frame. To achieve this, we need to better allocate time in our schedules for teamwork, bringing both efficiency and quality to our efforts to ensure financial responsibility for the project's outcome.

7.2 Four Principles

Below is a table that breaks down the four principles versus the broader context considerations.

	Beneficence	**Nonmaleficence**	**Respect for Autonomy**	**Justice**
Public Health, Safety, and Welfare	Ensuring the ReRAM-based architectures do not cause harm to the public through rigorous testing to ensure reliability.	Make sure the chip is designed to be electrically safe and will not overheat due to energy inefficiencies.	Empowering users to make an informed decision about whether they choose to use the product or not through documentation and tutorials.	Allowing all individuals to access this project and research through the use of the internet and documentation we have provided.
Global, Cultural, and Social	We have designed the tutorials and documentation to ensure that all classes through college can use and learn from our experiences.	The designs and practices through making these chips will not harm the users.	The design does not affect anything related to religion or culture.	Having the documentation presented online ensures that all social, cultural, and global communities will have fair access to this technology
Environmental	Developed to decrease energy consumption and reduce the environmental footprint and waste.	The production of one hundred chips will inevitably have an environmental impact due to the manufacturing process. However, in the long term, ReRAM technology is expected to contribute to smaller chip sizes and a reduction in energy consumption.	Our design, compared to other chips that are manufactured, will create an eco-friendly design due to reduced power consumption.	If the design works it will reduce the environmental footprint due to inefficiencies in chips globally.
Economic	The design will help create job	The design will not disrupt the	We provide four potential designs for	The implementation of ReRAM in chips

	opportunities due to the complexity and manufacturing process of the ReRAM cells.	economy, only help to improve AI implementation.	ReRAM-based architectures that will be allocated to any budget needs.	causes the creation of new markets, the generation of jobs, and the continuation of more sustainable practices throughout the economy.

Table 7.2: Four principles

One broader context-principle pair that is important to us is environmental beneficence. The primary purpose of this project is to reduce power from data going into the arithmetic logic unit and then back to the memory unit. This causes increased time, which correlates with an increase in power consumption. To ensure that this happens, we will utilize ReRAM's low-power characteristics and the CIM architecture to reduce the energy required for memory-intensive operations like MVM.

A context-principle pair that our final design will be lacking in the end but will not be prolonged is environmental nonmaleficence. When creating something out of theory, you need to test and recreate, and repeat the process until it is successful. At the end of April, this project will be sent to Efabless, and one hundred chips will be manufactured to be a test chip. This will cause a loss of materials and create waste from the manufacturing process. However, if this project shows promising results and grows in the future, it will reduce power consumption. Thus it will end up helping the environment and creating innovation in the other fields as well.

7.3 Virtues

Below are the three virtues that are important to this team.

1. **Clear and thorough documentation:** With the creation of something new, we have decided that one of our most important virtues was clear and thorough documentation. Clear and thorough documentation means that all design decisions, process findings, and project details are well-recorded. To portray that we are following this virtue, we have created tutorials and troubleshooting guides for the open software tools to help people follow in our footsteps. We are also documenting what errors we have run into with the architectures and what solutions we have come up with to overcome these challenges.

2. **Honesty:** Another one of our core virtues is honesty. This virtue correlates with our first virtue, stating that with clear and thorough documentation, we also need to be honest with our clients and the public about our errors and challenges. Honesty means being open and transparent about the issues and challenges we face when completing this project. To demonstrate our commitment to this task, we encourage open communication and try to maintain an environment where team members are comfortable discussing challenges or setbacks without fear of judgment. Any issues regarding timelines and setbacks are openly discussed during our weekly meetings and are addressed with an honest assessment and discussion.

3. **Cooperativeness:** Our last team member's core value is cooperativeness. This project has each member dedicating a certain amount of time that can be more extensive than other projects proposed. It also has a diverse set of technical skills needed to successfully implement the criteria into this project. Cooperativeness means working in a group collaboratively and supporting each other towards a common goal. We actively promote a team-first mentality, where successes and work ethic are recognized within the context of team collaboration. Regular work sessions are held to ensure that all team member's ideas are heard and have a chance to contribute to the designs.

Our individual core virtues are presented below.

- Sam Burns
    - Resourcefulness is one virtue I have demonstrated in my time spent on our senior design project so far. Resourcefulness is a crucial virtue when working through a project because it provides an opportunity to get access to materials and learn things that I wouldn't have known about; this opens the door to making more progress and developing a deeper understanding of the project. A couple of ways I have demonstrated this virtue are by meeting with various faculty with expertise outside that of our own project advisor and client, meeting with the 491 TAs, and reaching out to the Efabless community via their slack channel. Each of these resources helped me learn more about the skills required to succeed on our senior design project.

    - Patience is one of the most important virtues a team can demonstrate when working on a project. There have been times that I have felt frustrated with simulating results or unclear software errors. However, the key for a project to progress is remaining patient and dedicated to working through issues that arise. Every project will face struggles, remaining patient will only help the progress of a team. One way I can work to demonstrate this is taking more unique approaches to persistent issues I face in my circuit design on this project.

- Travis Jakl
    - Perseverance is a vital quality, especially in engineering and research projects, where challenges and setbacks are common. It helps me stay focused on long-term goals and motivates me to push through difficulties. By persevering, I can not only resolve issues but also learn valuable knowledge that improves my troubleshooting skills for this project and future ones. Perseverance helped me to push through the toolset errors I was receiving at the start of this project, utilizing documentation, former and current team members, and Slack to solve these issues. This not only helped myself, but helped my team as well.

    - Time management is essential for balancing multiple responsibilities and ensuring consistent progress on a project. I struggled with managing my time effectively as other coursework and commitments piled up, which led to challenges in

prioritizing tasks for the project. To improve, I plan to create a more structured approach by breaking the project into smaller, manageable tasks with clear deadlines. I'll use calendars and task lists to track progress and set aside specific time slots for focused work on the project. By regularly reassessing my workload, I'll ensure I stay on track and reach milestones without compromising the quality of my work.

- Noah Mack
    - Throughout our senior design project so far, I feel that I have demonstrated the virtue of perseverance. As a computer engineering student, I haven't had much experience with schematic creation and I have had no exposure to layout creation before this project. As we worked to get familiar with the open source tools, I kept trying even when things weren't working. However frustrating it was, I just needed to keep trying until I got it figured out. Perseverance is important to me because it is required for learning new things.
    - One important virtue that we haven't had the chance to demonstrate to its fullest extent is writing clear and thorough documentation. We did contribute to the ChipForge analog documentation as we worked through their tutorial, but for our project we will need detailed documentation so that our users have all of the tools they need to successfully utilize our test chip. This is an important virtue to me because I always appreciate when I am using a new technology and it has high quality documentation to streamline the learning process.

- Olivia Price
    - One of the virtues that is important to me is honesty. It is vital to communicate your successes and failures to your team so that they can help you or innovate on your work. I have demonstrated honesty by attending every weekly meeting and communicating the challenges I face or the solutions I have found. I have also asked questions when something is unknown to me or have voiced my concerns when the objective does not align with my knowledge.

    - One virtue that is also important to me is my lack of commitment to quality. Commitment to quality is crucial because it shows the client that they can trust me to maintain their satisfaction. It also improves efficiency, the project will gain a competitive advantage, and it will ensure long-term success. To demonstrate this virtue in the future, I will prioritize dedicating more time to the project and create a schedule that allows me to allocate additional hours for focused work.

8. Closing Material

8.1 Conclusions

So far our team has worked through the tutorials on the ChipForge website, gotten a newly designed inverter through the Efabless analog workflow, looked at the files from team sddec23-08, and begun making our own design choices for new ReRAM compute architectures. We have done background research on design choices in ReRAM arrays to back up our design choices and consulted with team sddec24-13 when deciding what peripheral circuitry to use. In addition, we have worked to update the analog workflow tutorials where we can. As for next semester, we will work to get both prior teams' designs through precheck within one digital harness. Additionally, we will integrate previously developed peripheral circuitry with the memory arrays of our own design to create two new architectures for characterization. Lastly, our final design will consist of all four architectures, along with a component testbench in a single digital harness that will be taken through precheck and tapeout check.

8.2 References

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8.3 Appendices

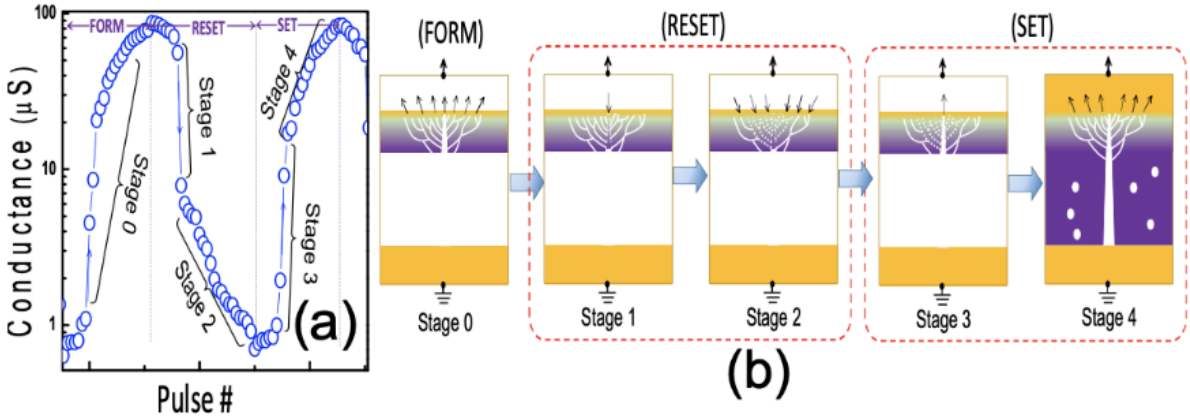

Fig. 10 After FORMing, the transition mechanism during RESET/SET can be divided into 4 stages. During FORMing, in Stage 0, a major filament with a wide radius and small filaments have developed. During RESET, in Stage 1, the major filament recesses and the conductance drops abruptly; in Stage 2, the small filaments slowly recess and the conductance drops gradually. During SET, in Stage 3. the major filament re-connects and the conductance jumps; in Stage 4, the small filaments re-connect and the conductance slowly increases.

Figure 8.1: explains ReRAM structural and operation basics and is extracted directly from [10]

Table 3 1T4R #9

1T4R #9	WL (V)	BL (V)	SL (V)	PW (ns)	Yield (%)
Pristine					100.00
Form	1.4 - 2.5 (0.1 step)	2.4 - 3.3 (0.1 step)	0	1000	99.80
Reset	2.5 - 3.0 (0.1 step)	0	2.4 - 3.0 (0.1 step)	1000	99.41
Set	1.7	2.4	0	1000	100.00

Alternative programming schemes can be used. For example, from our data on the 1T4R test #9 above, one could consider using a fixed reset pulse of WL=3V, SL=3V with a 1000ns pulse to ensure high RESET yields. Additionally, a lower voltage can be tried multiple times (e.g., a SET/READ and verify, or RESET/READ and verify) until the operation is successful. The pulse length is also a free variable, shorter (e.g., 100-200ns SET/RESET) pulses, with a verify scheme can also be used to reduce average write time.

Figure 8.2: explains ReRAM state change requirements and is extracted directly from [5]

9. Team

9.1 Team Members

- ➢ Computer Engineers
  - Noah Mack

- ➢ Electrical Engineers
  - Sam Burns
  - Travis Jakl
  - Olivia Price

9.2 Required Skill Set For Your Project

Below is a list of the required technical skill sets that are needed to complete this project successfully.

- Analog Design
  - Fabrication and Layout Design
  - Power Management and Efficiency
  - Circuit Simulation and Analysis
  - Measurement and Debugging
  - ReRAM Cell Architecture

- Digital Design
  - Synthesis
  - Logic and Circuit Design
  - Memory and Data Path Design
  - Hardware Description Design (Verilog)
  - Integration and Interface Design (C-code)
  - Testing and Debugging

9.3 Skill Sets Covered by the Team

Below is a table of skills that each team has acquired for this project, either during the semester or previously learned from prior semesters.

Skills	Team Member
Fabrication and Layout Design	All members
Power Management and Efficiency	All members

Circuit Simulation and Analysis	Sam Burns, Travis Jakl, & Olivia Price
Measurement and Debugging (Analog)	Sam Burns, Travis Jakl, & Olivia Price
ReRAM Cell Architecture	Sam Burns, Travis Jakl, & Olivia Price
Synthesis	Noah Mack
Logic and Circuit Design	All members
Memory and Data Path Design	All members
Hardware Description Design (Verilog)	Noah Mack
Integration and Interface Design (C-code)	Noah Mack & Sam Burns
Testing and Debugging (Digital)	Noah Mack

Table 9.1: Skill sets covered by team

9.4 Project Management Style Adopted By The Team

This team's project management was waterfall. Included in section 3.4 is our Gantt chart, which is a style of water project management. We divided the months across the two semesters into seven different tasks. Each primary task has one or two sub-tasks. We decided not to include hard deadlines because many of our functions depend on figuring out task one: how to use the open-source tools. Not much documentation is provided, so it will take time to acquire the knowledge on how to utilize them to their fullest capabilities.

9.5 Initial Project Management Roles

Below is the list of each team member and their acquired roles for this project.

- Sam Burns: Analog Signal Designer & Digital Signal Designer
- Travis Jakl: Analog Signal Designer & Digital Signal Designer
- Noah Mack: Digital Signal Designer
- Olivia Price: Analog Signal Designer

9.6 Team Contract

Team Name

_____SDMay25-19_____

Team Members:

1) _____Noah Mack_____ 2) _____Olivia Price_____

3) _____Sam Burns_____ 4) _____Travis Jakl_____

Team Procedures

1. Day, time, and location (face-to-face or virtual) for regular team meetings:
    a. Team meeting with advisors: Thursday, 2 pm, Durham 353
    b. Team meetings: Friday 1 pm, TLA, and Sundays 2 pm at ChipISU Club in Durham
2. Preferred method of communication updates, reminders, issues, and scheduling (e.g., e-mail, phone, app, face-to-face): Phone
3. Decision-making policy (e.g., consensus, majority vote): Consensus
4. Procedures for record keeping (i.e., who will keep meeting minutes, how will minutes be shared/archived): Meeting Notes will be kept on a running document in the shared google drive that has the rest of our collaborative resources.

Participation Expectations

1. Expected individual attendance, punctuality, and participation at all team meetings:
    Each person attends a set meeting. If attendance is not possible, then communication prior to the meeting is necessary.
2. Expected level of responsibility for fulfilling team assignments, timelines, and deadlines:
    Each team member maintains and holds their designated responsibilities, communicating progress and expected progress, as well as ensuring important tasks can be completed prior to deadlines
3. Expected level of communication with other team members:
    Communication should be clear and frequent. Communicate about problems, progress, or expected absences of meetings.
4. Expected level of commitment to team decisions and tasks:
    Each team member should be committed to their role and responsibilities, discussing any discrepancies with the rest of the team

Leadership

1. Leadership roles for each team member (e.g., team organization, client interaction, individual component design, testing, etc.):
    The proposed project will include one digital design member, Noah, while the rest will work on analog design. The client interaction will happen every week, face-to-face for an hour. This will include sharing out findings and whether the clients want what we propose. The individual component design will come down to Sam, Olivia, and Noah, while Travis coordinates between the three of us. This will ensure the analog and digital designs do not stray too far from each other.
2. Strategies for supporting and guiding the work of all team members:
    Travis will be the coordinator for digital and analog design. The goal of this project is to get all of the pieces of the FPGA board together. This involves knowing what everyone is doing and someone line streaming between us to keep us together.

3. Strategies for recognizing the contributions of all team members:

Team members will be responsible for making in-depth documentation of their work. Not only will detailed documentation make drafting the design document easier, but it will also allow members to efficiently keep track of their work.

Collaboration and Inclusion

1. Describe the skills, expertise, and unique perspectives each team member brings to the team.
    a. Noah - Deep knowledge of digital design and embedded C, can handle most of the surrounding digital architecture. Only computer engineering major on the team.
    b. Travis - Knowledge of both digital and analog design. This will be needed to integrate the analog and digital aspects of this project.
    c. Olivia - Electrical engineering with an emphasis in VLSI, which is designing and fabricating elements to be put on a board. This will help with putting the entire design together using analog and digital knowledge.
    d. Sam - Knowledge of analog circuit design and familiarity with digital schematic capture tools.
2. Strategies for encouraging and supporting contributions and ideas from all team members:

    Discuss all ideas from all team members; don't dismiss any ideas without exploring them first.
3. Procedures for identifying and resolving collaboration or inclusion issues (e.g., how will a team member inform the team that the team environment is obstructing their opportunity or ability to contribute?)

    Be upfront in communication. Be willing to bring something up to the group if it is bothering you. If truly uncomfortable with that, reach out to Professors or Advisors for help.

Goal-Setting, Planning, and Execution

1. Team goals for this semester:

Be prepared for the tapeout date of April 11, 2025. This involves having a working design that has been thoroughly simulated both in the digital tools and possibly on an FPGA to verify circuit behavior.

2. Strategies for planning and assigning individual and teamwork:

    When tasks/problems arise, discuss as a group how to distribute the workload, with a clear understanding of who is taking on what responsibility
3. Strategies for keeping on task:

    Assisting each other when problems arise, working in group settings with each other on the project, keeping each other accountable and on task

Consequences for Not Adhering to Team Contract

1. How will you handle infractions of any of the obligations of this team contract?

   The team discusses with the infractor their wrongdoings, and if no change occurs afterward, meet with advisors to discuss what further actions to take.

2. What will your team do if the infractions continue?

   Meet with the course/team advisors and discuss what further actions to take. If necessary, 4910 instructors will be involved if project advisors are unable to resolve the issue.

****

a) *I participated in formulating the standards, roles, and procedures as stated in this contract.*

b) *I understand that I am obligated to abide by these terms and conditions.*

c) *I understand that if I do not abide by these terms and conditions, I will suffer the consequences as stated in this contract.*

1) _____Travis Jakl_____ DATE _____9/13/24_____

2) _____Sam Burns_____ DATE _____9/13/24_____

3) _____Olivia Price_____DATE _____9/13/24_____

4) _____Noah Mack_____ DATE _____9/13/24_____