EE/CprE/SE 492 STATUS REPORT 6

4/4/2025 – 4/17/2025

Group number: SDMay25 - 19

Project title: ASIC Design of ReRAM-based AI Accelerators

Client &/Advisor: Dr. Wang, Dr. Duwe

Team Members/Role: Sam Burns (Mixed Signal designer), Travis Jakl (Mixed Signal Designer), Noah Mack (Digital Signal Designer), & Olivia Price (Analog Signal Designer)

- **Weekly Summary:**

This week, we made strides to get a top-level schematic for our design. After the many challenges we have encountered, we decided to shift our focus to what we can contribute to the overall design. We spent a lot of time testing and verifying components that were created in the past, so now it is time to put everything together. We worked on getting the previous team's architectures into usable formats for our top-level schematic. We also worked on the selection of results between each architecture.

In addition to working on our final design, we also put in a great deal of work on our design document. We read through every section, making note of what needs to be updated. Once we did this, we were able to have a successful meeting for our instructor meeting assignment.

- **Past week accomplishments**

• Sam Burns: I worked on identifying areas of the design document that would need to be updated, both in terms of work done this semester and as updates based on the situation with efabless.

• Travis Jakl: Continued to work on the testbench for the architecture select MUX, as well as implemented the updated schematic from team sddec23-08 into our top level. Also started to work on the design document.

• Noah Mack: I finished updating the schematic from team sddec23-08 so that its symbol is usable in our top level schematic. I also continued trying to get the sddec24-13 team's design simulated, but as we approach the end of the semester it is looking like we may need to shift our focus at this point. Also, a lot of time was spent working on our design document assignment for our instructor meeting.

• Olivia Price: Continued to work on getting simulating test benches and components in order to give a demonstration at the end of the semester. Also started to work on the design document.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Sam Burns	Went through design document identifying which areas would need	6	84
Travis Jakl	Implemented sddec23-08 design into top level, continued working on testbench for architecture select, worked on design doc	7	72
Noah Mack	Continued working on sddec24-13 testbench. Finished new schematic for sddec23-08 design. Worked on design doc.	6	84
Olivia Price	Continued to work on the testbench for the 4-bit ADC from the prior team, and also worked on the design document.	15	62

- **Plans for the upcoming week**
  - Sam Burns: Begin to work on the final version of the design document, make visuals that will be used for the design document and poster as well. Also work on the presentation for IRP.
  - Travis Jakl: Finish the architecture select testbench, add top-level schematics and testbenches to the design document. Work on the poster and our presentation.
  - Noah Mack: Help with any simulations or designs that still need to be finished up, then start focusing on final deliverables like our poster and design document.
  - Olivia Price: Continue to work on the 4-bit ADC testbench and focus on the final deliverables. Hopefully, these simulations will work, so we have more content to add to our testing sections and have content for our demonstration video.

- **Summary of weekly advisor meeting**

In our weekly meetings for this timeframe, we talked a lot about what our final deliverables are going to look like, both design and documentation. We are nearing the end of the semester, so it is time to start bringing everything together. For the design, we decided to work with what we have and hopefully come up with a top-level schematic that can select between different architectures, as well as have accessible individual component circuitry. On the documentation side of things, we discussed updates that need to be made for our design document, and Dr. Duwe gave us some insight into what our poster should look like.