EE/CprE/SE 492 STATUS REPORT 5

3/13/2025 – 4/3/2025

Group number: SDMay25 - 19

Project title: ASIC Design of ReRAM-based AI Accelerators

Client &/Advisor: Dr. Wang, Dr. Duwe

Team Members/Role: Sam Burns (Mixed Signal designer), Travis Jakl (Mixed Signal Designer), Noah Mack (Digital Signal Designer), & Olivia Price (Analog Signal Designer)

- **Weekly Summary:** This week, our primary focus has been finalizing the schematics and working towards producing meaningful simulation results. Achieving this milestone is crucial, as it will enable us to seamlessly integrate the top-level designs into our own system. By ensuring that our schematics function as expected, we can confidently move forward with implementation and further testing. In parallel, we have also begun updating our design documentation to reflect our latest progress. This includes refining technical details, troubleshooting common challenges, and outlining key design considerations. Additionally, we are developing comprehensive tutorials and guides to assist future team members in understanding and replicating our work. These resources will serve as a valuable reference, ensuring continuity and knowledge transfer within the team.

- **Past week accomplishments**

  • Sam Burns: Worked on the top level testbench for the sddec23-08 team's final design so that it can be tested separately from our top level design.

  • Travis Jakl: Worked on the top level schematic for our final design, including our peripheral circuitry, ssdec24-13 final design, ssdec23-08 final design, and our architectures as well.

  • Noah Mack: I have still been working on getting the sddec24-13 team's final design testbench through simulation. We gained a little bit of insight through meeting with a member of their team, so I am hoping to be able to get that done soon. As we work towards integrating our final design, I have started work on adapting the sddec23-08 team's top level schematic so that it is usable as a subcomponent of our top level design..

  • Olivia Price: For the last three weeks, I have worked on the comparator testbench to get it to work. Luckily, it works now. I also attended a meeting with a member of the previous team and learned about discrepancies between their toolchain and ours. This is the reason why most of their test benches seem to not work. I also started to create a top-level testbench from a prior team.

- **Individual contributions** *(*

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Sam Burns	Worked on sddec23-08 top level testbench	6	72
Travis Jakl	Created our top level design for the most part	7	72
Noah Mack	Continued working on sddec24-13 testbench. Started working on adapting sddec23-08 schematic for our top level design.	6	72
Olivia Price	Created a new comparator testbench and proceeded to get it to work. Started on creating a testbench for the top-level design for a prior team.	10	42

- **Plans for the upcoming week**
  - Sam Burns: Continue working on the sddec23-08 testbench, and work on the design document to start getting it updated.
  - Travis Jakl: Finalize our top level schematic, and then work towards creating macros for our peripheral circuitry in order to effectively produce a layout for it.
  - Noah Mack: Keep working on sddec24-13 final schematic and finish up the pins for the sddec23-08 schematic.
  - Olivia Price: Continue to work on the prior team's top-level testbench. After that, we will be able to integrate our different designs into their top-levels and test them. Then, this will give us simulations to provide feedback on which design looks promising for the research test vehicle.

- **Summary of weekly advisor meeting** (*If applicable/optional)*

During our meeting, we reviewed our discussion with a former team member and discovered that they had downloaded their tools individually rather than using a standardized toolchain. This discrepancy introduced errors in the previous team's schematics and test benches. As a team, we had been struggling to understand why their test benches consistently produced errors during our simulations, despite their assurances that everything had worked on their end. The missing context regarding their tool setup had been a major source of confusion. However, after identifying this issue, we finally understood why we had been encountering so many unexpected errors. After talking with our advisor, he said to try and get the top-levels to simulate.