EE/CprE/SE 492 STATUS REPORT 3

2/27/2025 – 3/13/2025

Group number: SDMay25 - 19

Project title: ASIC Design of ReRAM-based AI Accelerators

Client &/Advisor: Dr. Wang, Dr. Duwe

Team Members/Role: Sam Burns (Mixed Signal designer), Travis Jakl (Mixed Signal Designer), Noah Mack (Digital Signal Designer), & Olivia Price (Analog Signal Designer)

- **Weekly Summary:** During the last two weeks, the team has been working on simulating components and top-level schematics from the previous teams. Most schematics have simulation errors that take quite a while to troubleshoot. However, our goals for the project have changed due to Efabless ceasing fabrications and closing their company. As of now our goals are mostly the same, but we will not have a fabrication date, which gives us more time to finish the project. However, we will lose the experience of getting a chip to the point where it can be fabricated.

- **Past week accomplishments**
  - Sam Burns: Worked on creating testbenches for team sddec23-08 op amps and high level circuit.
  - Travis Jakl: Worked on cleaning up the troubleshooting notes for the project, as well as gathering the information from our slack posts and adding those to documentation as well
  - Noah Mack: Continued work on the sddec24-13 final schematic. After trying a lot of different things, I finally tried to just let the simulation go and it ran for about 20 minutes but I was able to get some error output that showed some issues with the spice script. This will require some adjusting, but I think I will now shift my focus to individual components to make sure we get all of those ready for our final schematic by the deadline.
  - Olivia Price: The comparator is still not simulating from one of the past team's designs. I made a new testbench for it using inspiration from a comparator testbench that was already made by the sky130nm process. Hopefully I can troubleshoot a lot over spring break and get it to work, and be done with it.
- **Pending issues**
  - Sam Burna: Got an error in simulation that no one has been able to resolve yet. Getting support for this may be difficult due to the efabless slack shutting down soon.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Sam Burns	Created testbenches for sddec23-08 top level schematic and two different op amps used in their design	6	60
Travis Jakl	Cleaned up troubleshooting documentation and added slack information	7	20
Noah Mack	Simulating FinalSch.sch from sddec24-13	6	60
Olivia Price	Troubleshooting the comparator until it works. Looking at ways to test noise on the components to see where the thresholds lie and how to mitigate noise.	6	32

- **Comments and extended discussion**

  I feel disheartened that efabless shut down.

- **Plans for the upcoming week** *(Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.)*

  • Sam Burns: I will work on the top level testbench for team sddec23-08. If time allows I also hope to start doing more advanced testing of op-amp performance characteristics.

  • Travis Jakl: Slack is shutting down in the near future, so I will work on gathering as much of our slack information, as well as the previous teams slack information as possible.

  • Noah Mack: I will shift my focus to individual components and explore the process of using Verilog to test components. I will look at previous team's documentation and code to help with this.

  • Olivia Price: Finish troubleshooting the comparator, then move on to creating schematics for our design. Also going on a sidequest to see if I can get noise to simulate in the components using the Gaussian function over spring break which can help us mitigate some of the risks.

- **Summary of weekly advisor meeting:** In our recent meeting, we discussed the impact of Efabless's shutdown on our project. Efabless has ceased operations due to funding challenges, affecting our project that relied on their services. We evaluated which of our goals remain achievable and which are now uncertain. As Senior Design II nears its end, we emphasized the importance of documenting our experiences and insights. Building on the previous team's work, we plan to create tutorials to guide future teams. For example, developing a step-by-step guide on

running a design through pre-check processes would be beneficial. This documentation will ensure that our knowledge is preserved and can serve as a valuable resource for those who continue similar projects in the future.