EE/CprE/SE 492 STATUS REPORT 3

2/13/2025 – 2/27/2025

Group number: SDMay25 - 19

Project title: ASIC Design of ReRAM-based AI Accelerators

Client &/Advisor: Dr. Wang, Dr. Duwe

Team Members/Role: Sam Burns (Mixed Signal designer), Travis Jakl (Mixed Signal Designer), Noah Mack (Digital Signal Designer), & Olivia Price (Analog Signal Designer)

- **Weekly Summary** For the last two weeks, the team has been working on getting components through simulations, layout, design rule checks, layout versus schematic, precheck, and tapeout checks. Last week, a few members of our group engaged in a discussion with Efabless about the process of integrating both digital and analog components onto a single chip. We explored various approaches and strategies for fabricating mixed-signal chips that combine digital circuitry for processing and analog circuitry for handling real-world signals.

- **Past week accomplishments**

  • Sam Burns: Attended a meeting with Efabless staff and learned about compatibility issues with our current design and the wrapper being used. Then I started putting together some resources about how we can approach this issue.

  • Travis Jakl: Attended meeting with Efabless staff. Worked through issues regarding a digitally synthesized module in our analog wrapper and worked on getting wrapper through precheck.

  • Noah Mack: Continued working on FinalSch.sch by creating new symbols for components that used inverters after we switched to the previous team's inverters which include VDD and VSS connections. Needed to create new symbols and replace them in the schematic. Also began investigating openlane/mixed-signal design with the digital wrapper after Sam and Travis attended their meeting and discovered some new information.

  • Olivia Price: Proceeded to get the two-stage operational amplifier through design rule check-in layout. Still struggling with getting the comparator to simulate in xschem. However, I have been talking to slack to try and resolve this problem.

- **Pending issues** *(If applicable: Were there any unexpected complications? Please elaborate.)*

  • Sam: The analog wrapper does not surrport digital standard cells, this will make it so a design cannot be taped out. We need to investigate the digital wrapper, that supports mixed signal designs, and learn how to use our analog components inside it.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Sam Burns	Attended meeting with efabless staff and investigated issues related to the digital wrapper with mixed signal designs	6	48
Travis Jakl	Attended meeting with Efabless staff. Worked through issues regarding a digitally synthesized module in our analog wrapper	6	49
Noah Mack	Updated some symbols/schematics that needed VDD and VSS connections within FinalSch.sch. Began investigation of openlane and mixed-signal design.	6	48
Olivia Price	Got the two-stage op-amp to pass the design rule check. Troubleshooting the monte carlo simulation in order to get it to work.	7	26

- **Plans for the upcoming week** *(Please describe duties for the upcoming week for each member. What is(are) the task(s)?, Who will contribute to it? Be as concise as possible.)*

  • Sam Burns: I plan to work on the simulation and verification of the top level schematic for team sddec23-08

  • Travis Jakl: Finalize the troubleshooting with the digitally synthesized module in analog wrapper, document the resolution to the issue, and continue to get important modules through precheck

  • Noah Mack: Continue investigating openlane and start trying to create some verilog modules that we will need.

  • Olivia Price: Continue to troubleshoot the Monte Carlo simulation in Xschem and hopefully figure out the problem. Then start running simulations on the top-level circuit in xschem and debug that as well.

- **Summary of weekly advisor meeting** As the fabrication deadline approaches, we have decided to refine our focus and concentrate on our primary objective. Rather than attempting to develop a circuit that reduces power consumption while using AI, we will prioritize integrating both analog and digital components onto the same chip using a fabrication process that is not yet documented. By doing so, we aim to provide a solid foundation for those who follow us, allowing them to concentrate on the design of the ReRAM AI accelerator, without having to worry about the underlying tools and fabrication procedures. That being said, this chip will also serve as a test vehicle. We will need to implement a system that allows users to test individual components, enabling them to identify what is functioning properly and what may need adjustments.

Fabricating this chip will not only guide future teams in the right direction but also provide them with a head start, allowing them to build on our final deliverable and progress more efficiently.