EE/CprE/SE 492 STATUS REPORT 1

1/21/2025 – 1/28/2025

Group number: SDMay25 - 19

Project title: ASIC Design of ReRAM-based AI Accelerators

Client &/Advisor: Dr. Wang, Dr. Duwe

Team Members/Role: Sam Burns (Mixed Signal designer), Travis Jakl (Mixed Signal Designer), Noah Mack (Digital Signal Designer), & Olivia Price (Analog Signal Designer)

- **Weekly Summary:** For the last two weeks, we have been working on getting specific aspects of the fabrication criteria to work. This means getting an analog part through pre-check and tape out on eFabless servers. Also, the team is going through past teams' designs and seeing which ones work and which ones need some further troubleshooting. As a team, we have run into a lot of troubleshooting issues where past team designs have some bugs in them.

- **Past week accomplishments**

  • Sam Burns: I worked on learning the efabless hosted precheck and tapeout check processes on a part that had passed local precheck. I was able to successfully get a component through both jobs, while identifying the minimum files necessary to do so. I also worked to fix file path issues.

  • Travis Jakl: Worked on getting the 2-1 mux layout fixed and through local precheck, then began working on 4-1 mux layout and post layout simulations.

  • Noah Mack: I have been working on ensuring that our Git repo can properly accommodate our workflow. I have been setting up relative paths for symbols in our xschem schematics and trying to run simulations. I ran into some issues with the ngspice files that were present in our dependencies folder, but I seemed to be able to fix these by reinstalling the pdk and copying the files over to the repo. Now I am in the midst of attempting to simulate the final schematic from team sddec24-13 from inside of the git repository.

  • Olivia Price: I reviewed and debugged various components developed by the previous team, thoroughly analyzing each one for functionality and performance issues. After identifying areas that needed improvement, I documented whether each component was fully operational, partially functional, or non-operational.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Sam Burns	Successfully passed component through Efabless hosted precheck and tapeout jobs	6	38
Travis Jakl	Got components through local precheck	7	38
Noah Mack	Worked on Git repo (see above)	6	36
Olivia Price	Continued to debug previous teams' components and document whether they worked or not.	6	19

- **Plans for the upcoming week**

  - Sam Burns: In the upcoming week I will work on simulating the top level designs of both teams schematics, and debugging any issues that arise. I will also be testing individual components as well

    • Travis Jakl : Worked on getting components through local precheck, simulating components, and doing layout in magic

    • Noah Mack: Simulate FinalSch.sch from our repo and then continue documenting part status.

    • Olivia Price: Continue to document whether components work or not from previous teams. Hopefully, start on load analysis, which would entail putting a capacitor on the output of the component and see if it still functions properly.

- **Summary of weekly advisor meeting:** This week, during our team meeting, both the advisor and client expressed concerns regarding the testing of our designs, particularly in relation to ensuring optimal performance when the components are fabricated. They raised valid points about how certain components might behave differently once they are integrated with others, as opposed to when they are tested individually. To address these concerns and ensure the reliability of the components when assembled, we plan to conduct stress testing on the individual components once they are attached to others. Specifically, one of us will simulate real-world conditions by attaching loads and capacitors, estimating the expected load for each component. This will allow us to observe how the components perform under stress and whether they still function according to the intended specifications.