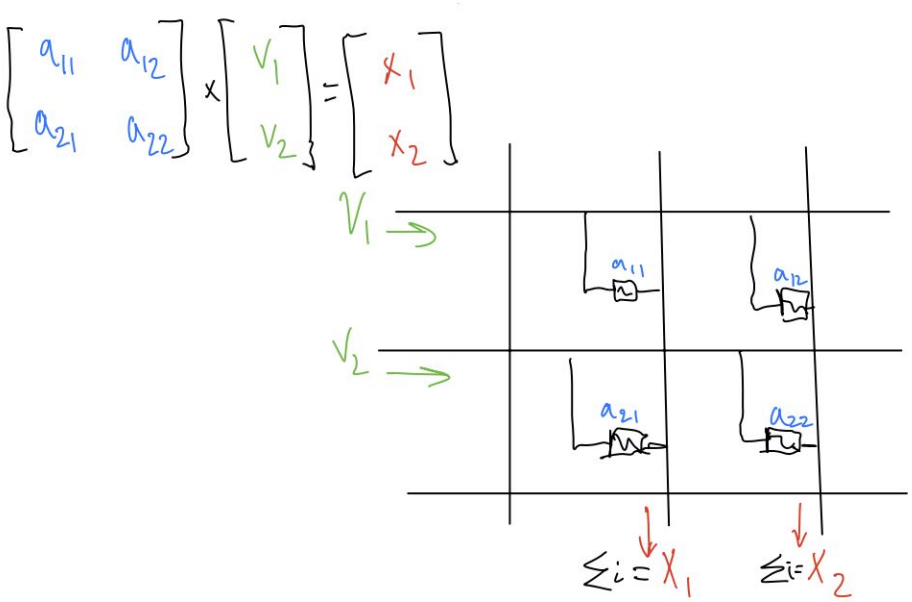
ASIC ReRAM AI Accelerator

User Needs and Requirements

By: Noah Mack, Olivia Price, Travis Jakl, Sam Burns

Project Overview

- **ReRAM-based AI Accelerator ASIC Design**
  - ReRAM is emerging non-volatile memory technology
  - Not many opportunities exist for fabrication
  - Research Vehicle (Will Include Multiple Architectures)
- **In-memory matrix-vector multiplication**
  - Performs calculations in the analog domain by adding currents (think KCL)



User Needs

Primary Client Need (Professor Duwe):

- Hoping to minimize the power used by the chip by making matrix multiplication in the ReRAM cells
- Looking for a research vehicle to perform testing based on different architecture layouts
- Wants to have four different layouts that work with ReRAM cells

User Needs

Secondary Users Needs (ChipForge and Graduate/undergraduate students):

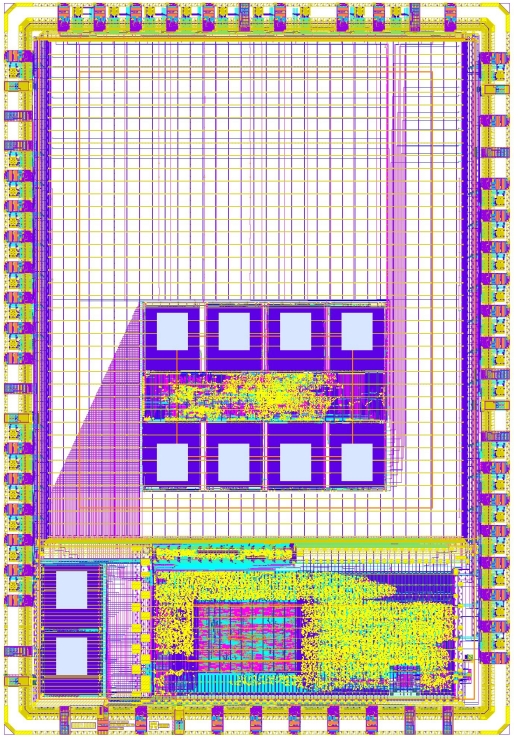
- Tutorials for the analog side on how to use the tools
- Troubleshooting documentation

Tertiary Users Needs (Public):

- Documentation for how to get started using the analog flow of xschem, netgen, NgSPICE, and magic
- Design documentation saying how we designed our circuits, and how matrix multiplication works with ReRAM cells

Requirements

- **Functional:**
  - Follow Skywater 130nm process
  - Final design pass pre-check before **April 11th**, which will then be fabricated at efabless
  - 4 architectures for user to select from
  - Bring-up code
  - Peripheral circuitry testbenches
- **Resource:**
  - Overview of design choices and architectures
  - **Bring-up documentation**
  - Uncertainty evaluation



Engineering Standards

- **IEEE 1481-2019- IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA):** This is applicable to our project since it specifies how our integrated circuit should be examined using a variety of design automation tools for timing and power consumption.
- **IEEE 1076.4-2000- IEEE Standard VITAL ASIC Modeling Specification:** This standard is relevant to our project because it calls for the testing of an ASIC chip using extremely precise and effective simulation models.
- **IEEE 1149.4-2010- IEEE Standard for a Mixed-Signal Test Bus:** This is relevant to our project since it will have both digital and analog components, and we will need to properly test each one separately and in tandem.
- **IEEE 1364-2005- IEEE Standard for Verilog Hardware Description Language:** Since our project requires us to create Verilog code to facilitate communication between the wrapper and the analog portion, this standard is appropriate for us.

Conclusion

- Research vehicle for in-memory computation
- Varying users and user needs
- Many functional requirements, less resource requirements
- IEEE standards

Average ReRAM hater