Project Planning

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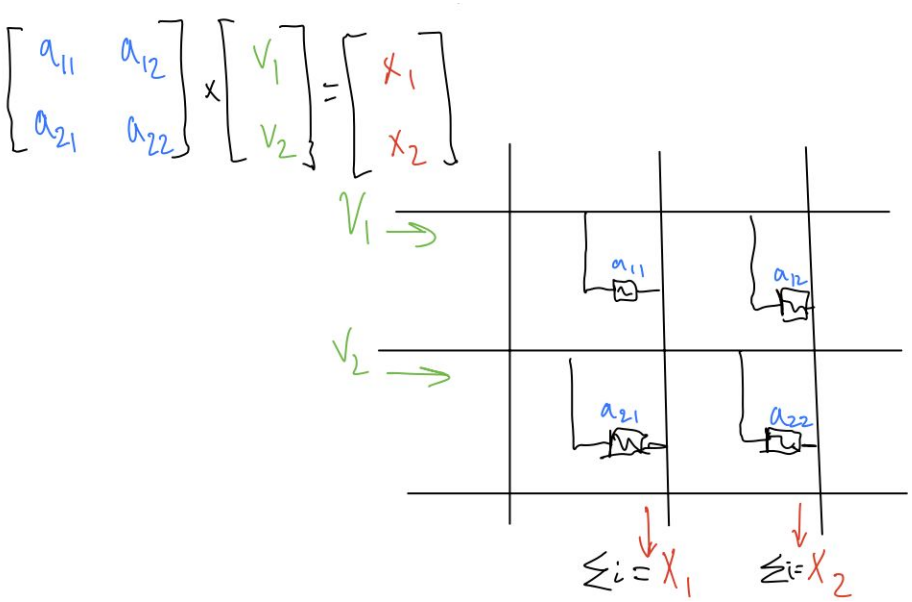
SDMay25-19

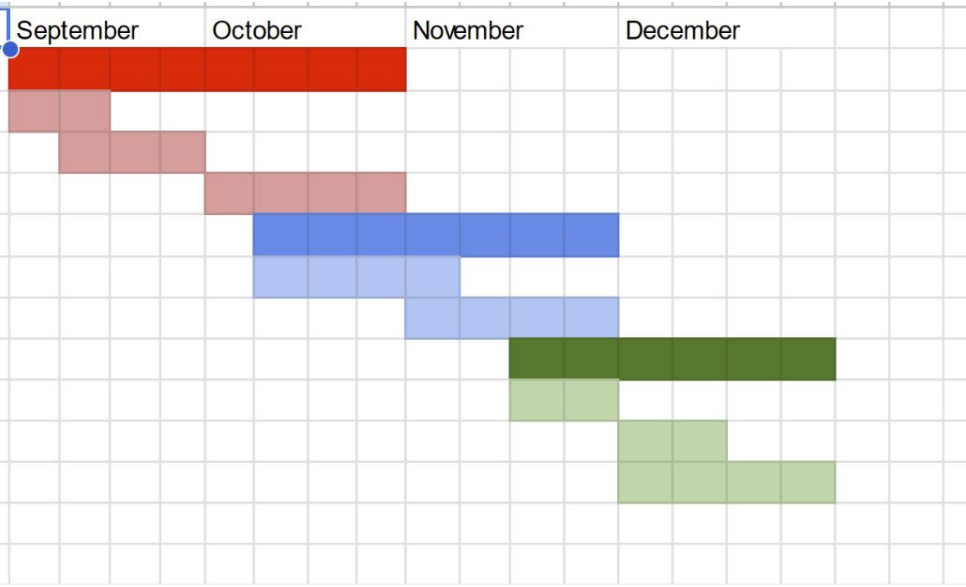
Project Overview

- **ReRAM-based AI Accelerator ASIC Design**
  - ReRAM is emerging non-volatile memory technology
  - Not many opportunities exist for fabrication
  - Research Vehicle (Will Include Multiple Architectures)
- **In-memory matrix-vector multiplication**
  - Performs calculations in the analog domain by adding currents (think KCL)



Gantt Chart

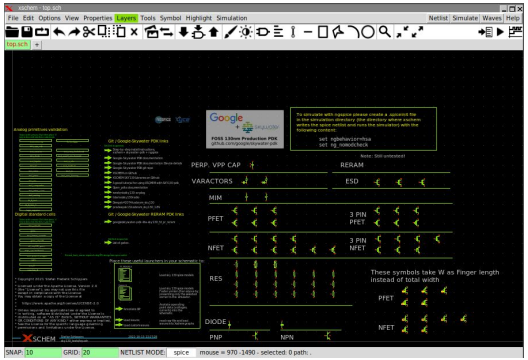
Task Decomposition	September	October	November	December
Task 1: Figure out the tools				
Installing toolchain				
Following tutorials				
Get an analog device through Pre-check				
Task 2: Verify and integrate previous architectures and peripheral circuitry				
Looking at other team's components and testing if they work				
Get the other team's components through pre-check				
Task 3: Research and implement new architures				
Create schematic for new architecture #1				
Create schematic for new architecture #2				
Implement new architectures into top-level design				

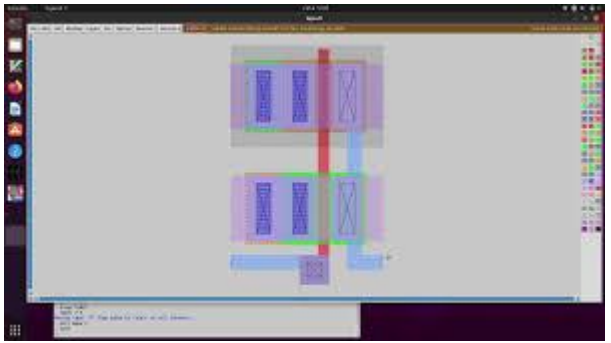


Task Decomposition

Task 1: Figure out tools

- Install toolchain and follow tutorials
- Make an inverter using xschem and magic
- Get an analog devices through pre-check
    - Pre-check allows us to see if the design will be able to be fabricated into a chip

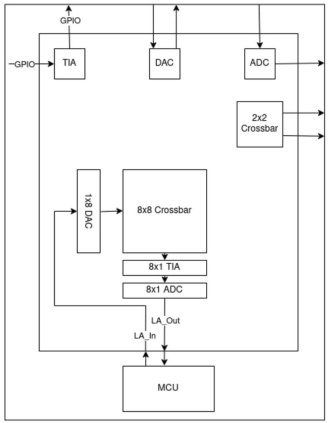




Task Decomposition

Task 2: Verify and integrate previous architectures and peripheral circuitry

- Looking at previous teams designs
  - Checking to see if they work properly, by creating testbenches for them
  - Checking to see if all of their components are working correctly and pass pre-check
    - If they do not pass pe-check then fix them to pass pre-check



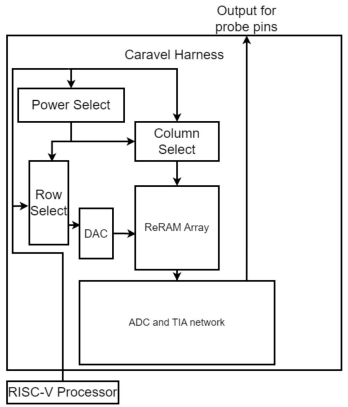


Figure 5: General Diagram for the overall design

Task Decomposition

Task 3: Research and implement new architures

- Create a new schematic #1
  - Gather components from past teams and create a new schematic with various components from different designs and incorporating new innovations from our team
- Create a new schematic #2
  - Gather components from past teams and create a new schematic with various components from different designs and incorporating new innovations for our team to contribute too
  - Design will be different from schematic #1

Key risks/mitigation

The main risk include:

- Four different architectures
  - The four architectures need to pass through pre-check
  - Everything must have testbenches and there must be C-code interface
- Design will need to be handed in by April 21st and must be able to be fabricated according to efabless standards.

In order to fulfill our requirements we need to follow the timeline of our gantt chart, and communicate as a team. Play to each others strengths. Problem solve early and often with the tools, so we do not run into user error during second semester.

Conclusion

Task decomposition:

1. Figure out tools
2. Verify and integrate previous architectures and peripheral circuitry
3. Research and implement new architures

Main Risk: Not getting a fully functional design to turn into eFabless by April 21st

Risk Mitigation: Stick to the plan and communicate if someone needs help.