Detailed Design

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Project Overview

Our project focuses on creating a ReRAM-based compute-in-memory (CIM) test chip to improve matrix-vector multiplication efficiency in machine learning. Traditional CPUs struggle with the data bottleneck and energy cost of constant data movement, so our design incorporates multiple ReRAM architectures to enable parallel computation directly in memory. We'll fabricate the chip using the Skywater 130nm process, allowing ISU researchers and ChipForge club members to test and analyze different ReRAM designs. Alongside the chip, we'll provide documentation and C code for interfacing, helping research teams evaluate CIM's potential in low-power computing.

Design

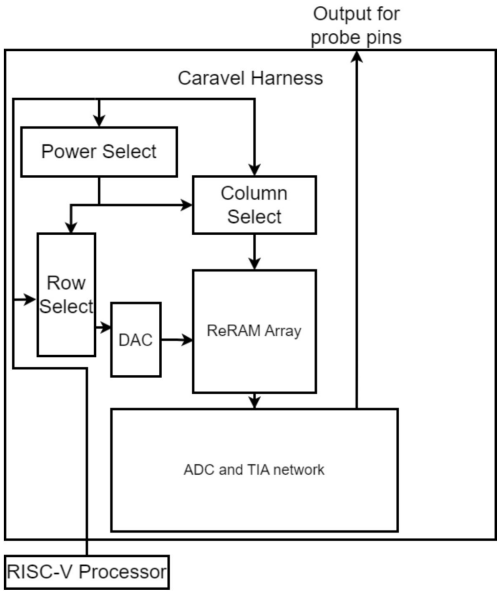
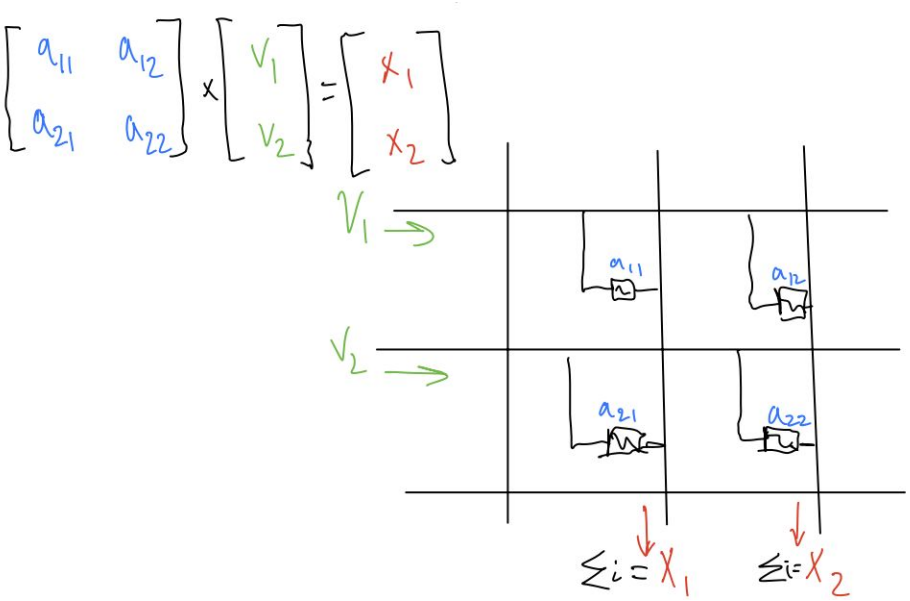


Figure 5: General Diagram for the overall design



Functionality

Setup and Initialization:

- User powers up the chip and connects it to an MCU.
- Configures the ReRAM architecture via C-based commands.

Running Tests:

- Initiates matrix-vector multiplication operations directly in ReRAM.
- Achieves energy-efficient, parallel computation by minimizing CPU-memory data transfers.

Data Collection and Analysis:

- Captures performance metrics (e.g., power, speed, error rates) through the MCU.
- Allows for real-time observation or data saving to compare architecture performance.

Iterative Testing:

- User switches between architectures as needed.
- Enables detailed testing and characterization of each ReRAM design.

Technology Considerations

Software used:

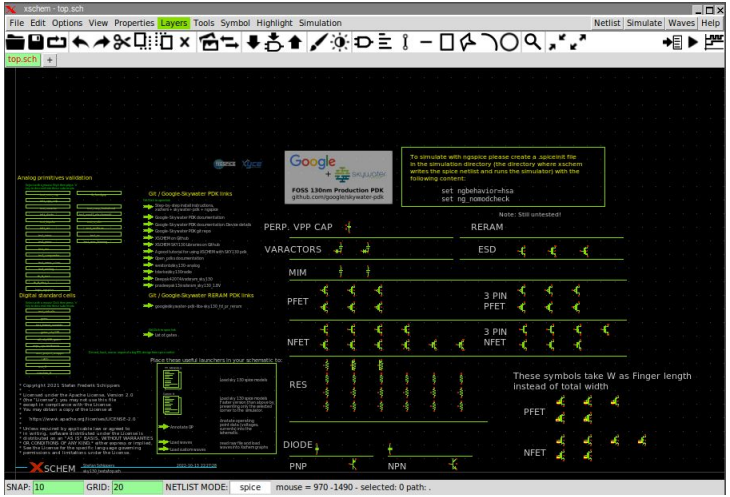
- Xschem
- Magic
- Netgen

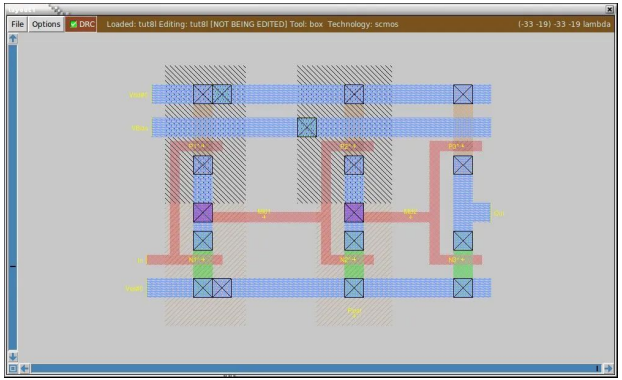
Benefit: All software used for this project is open source

Drawback: Learning curves to get familiar with software

Design Alternatives:

- Reuse of previously developed peripheral components
- Open sourced documentation of component designs





Areas of Concern and Development

- Proposed design satisfies all current requirements

Primary Concerns:

- Noise on analog lines
- Function of peripheral circuitry
- Support from the open-source-silicon Slack channel

Conclusions

In summary, our ReRAM-based compute-in-memory (CIM) test vehicle provides a platform for evaluating matrix-vector multiplication performance in a low-power, parallel computing environment. By incorporating multiple ReRAM architectures, our design allows ISU researchers and students to explore and characterize each architecture's unique attributes. The project leverages open-source tools and the Skywater 130nm process to make fabrication feasible, with documentation and interfacing code that support testing and analysis. Successfully meeting our tapeout goal will contribute valuable insights to CIM research, paving the way for more energy-efficient computing solutions.